Welcome To

ISSCC 2014 Session 28 Mixed-Signal Techniques for Wireless

A Programmable 0.7-to-2.7GHz Direct ΔΣ Receiver in 40nm CMOS

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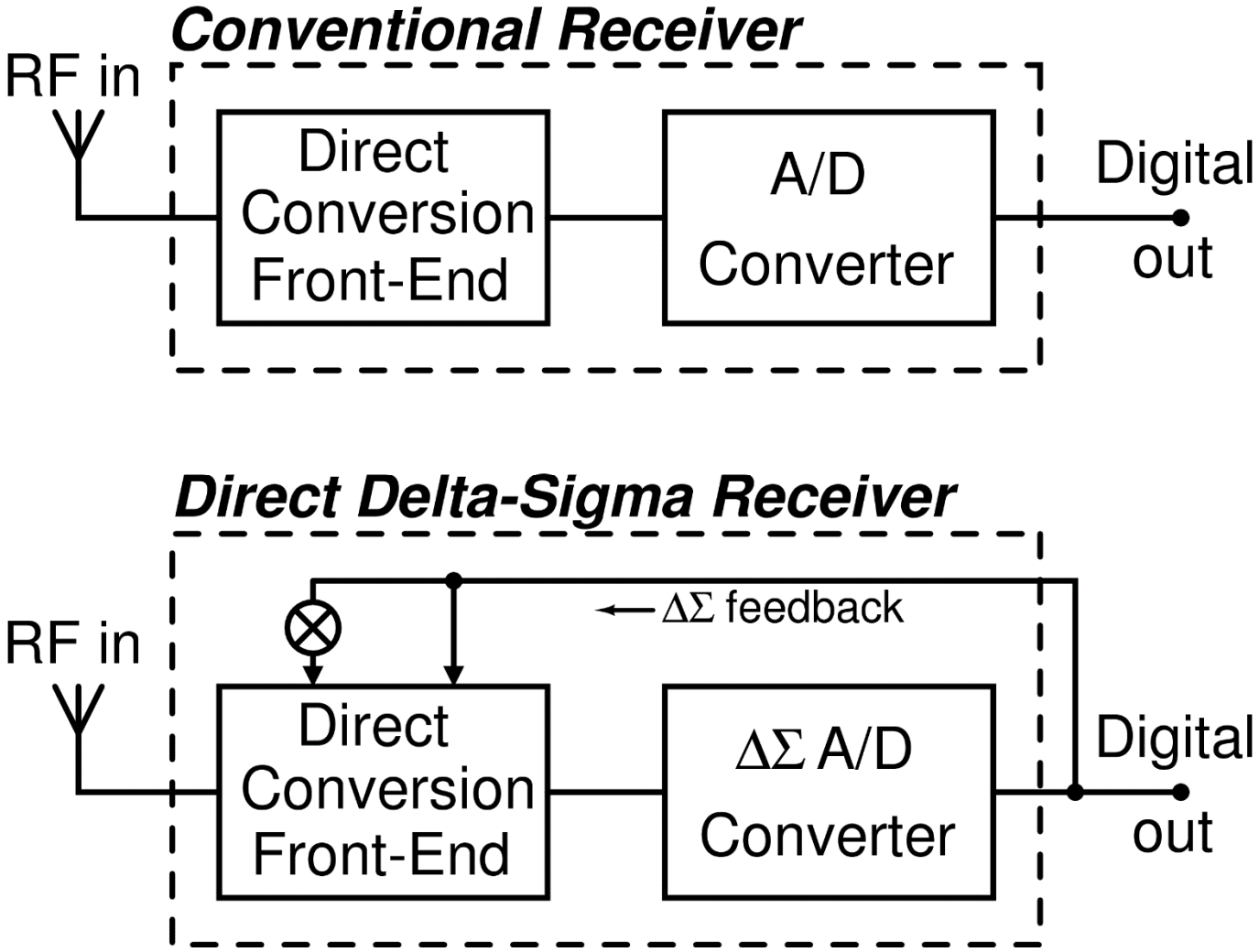
Outline

- General DDSR overview
- RF section
- Baseband section
- Experimental results
- Conclusions

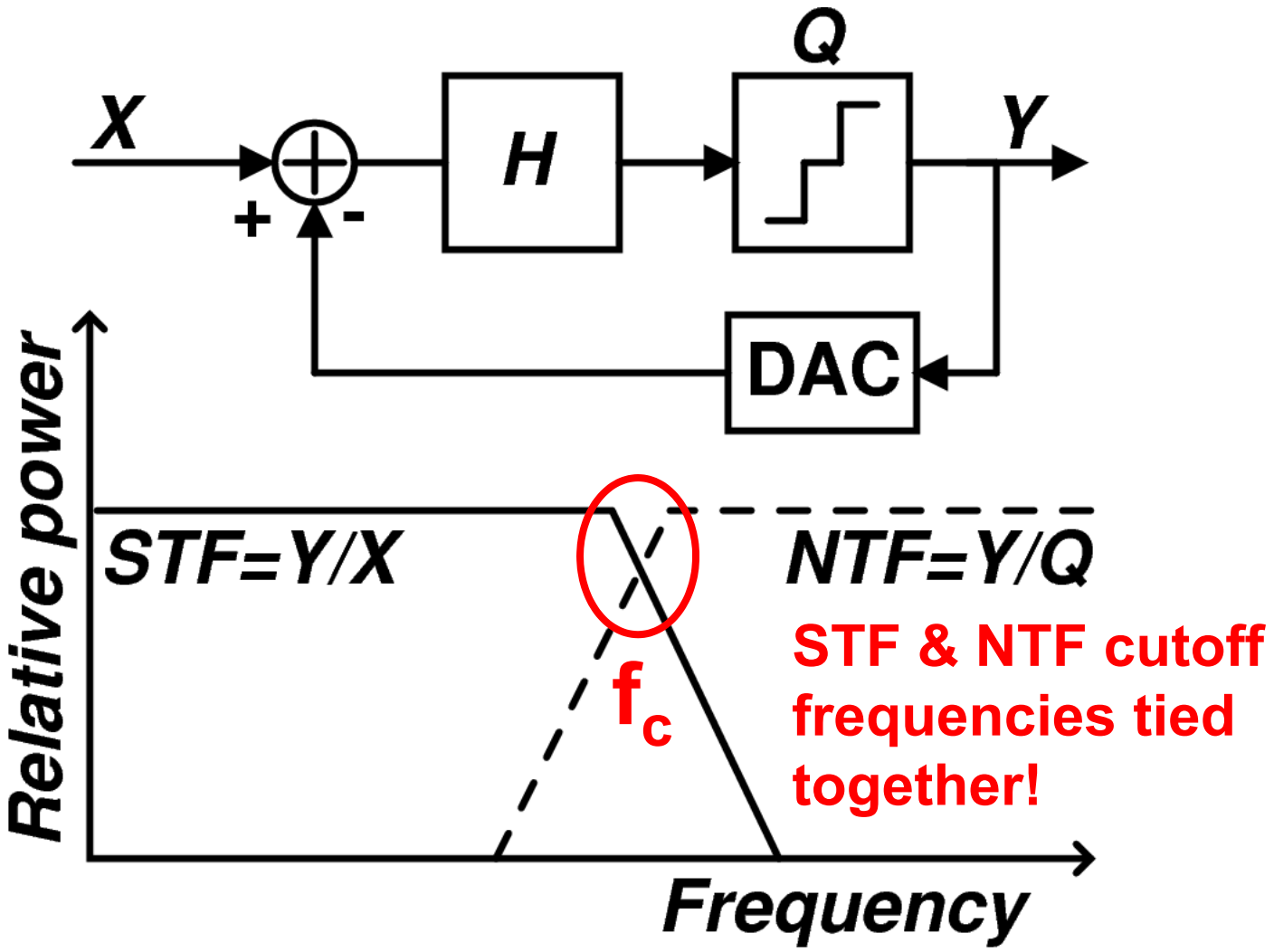
General DDSR Overview



Koli et al., *ISSCC 2010*

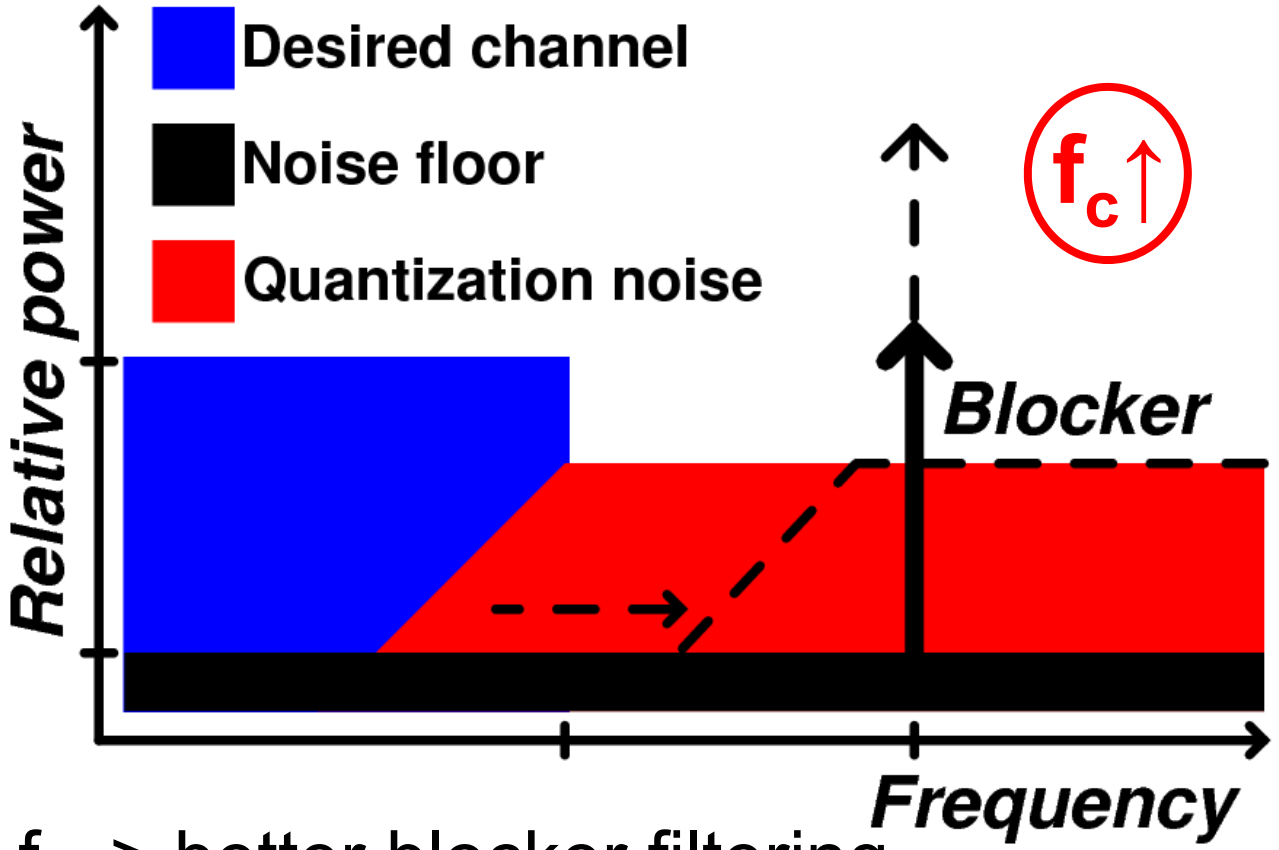
General DDSR Overview

ΔΣ ADC



General DDSR Overview

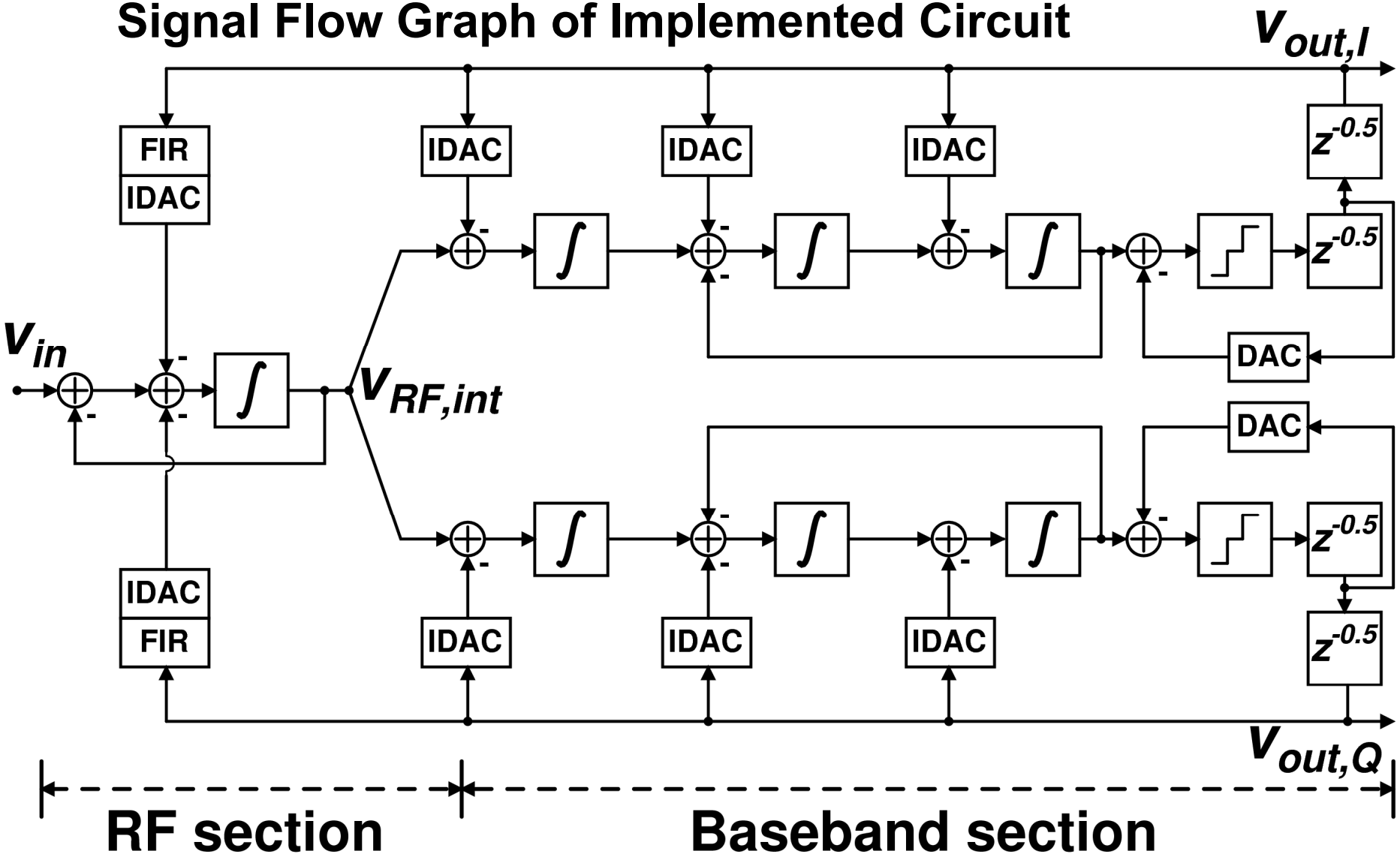
Simultaneous Channel Filtering and Noise Shaping



- Low f_c -> better blocker filtering
- High f_c -> better noise shaping

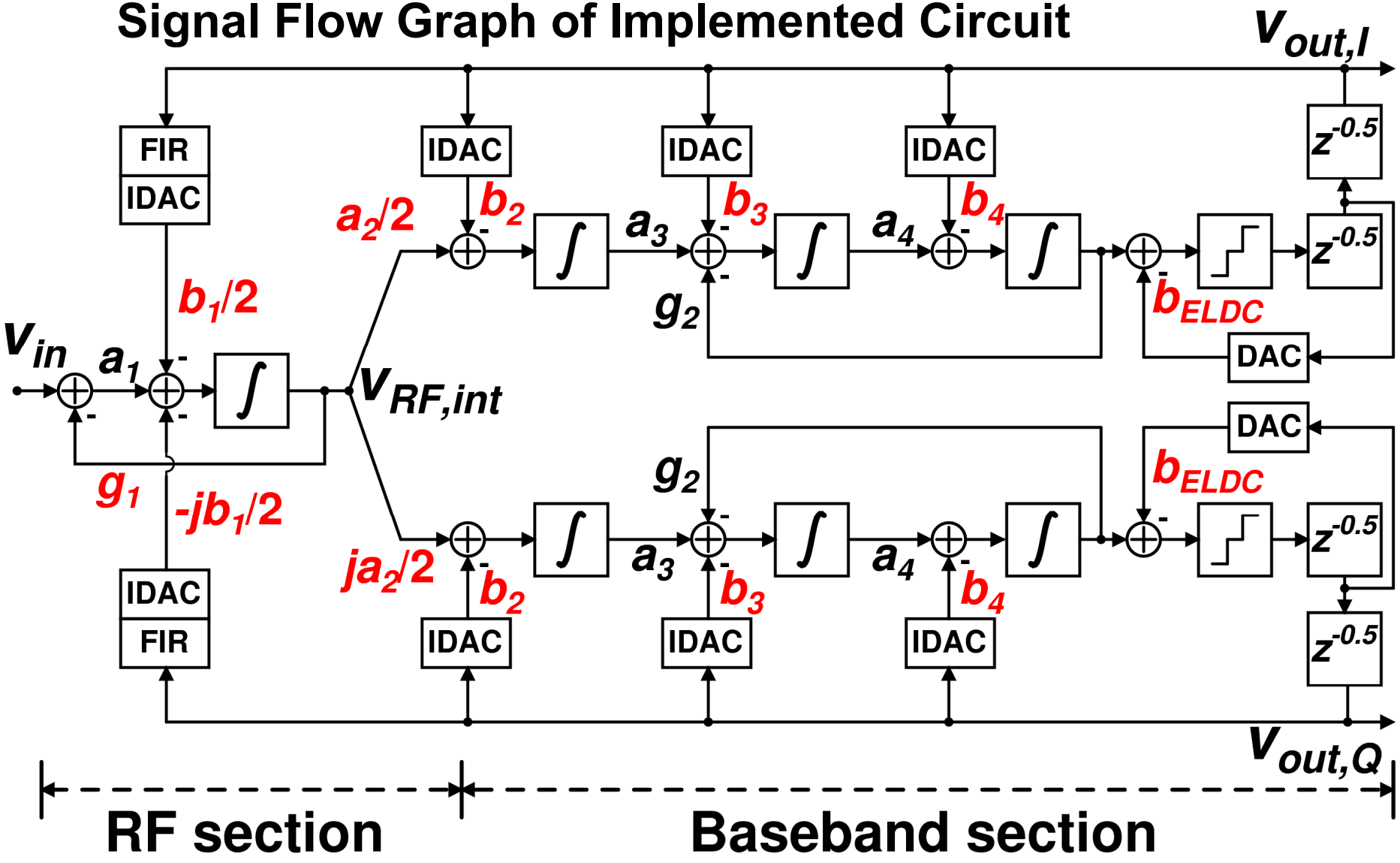
General DDSR Overview

Signal Flow Graph of Implemented Circuit



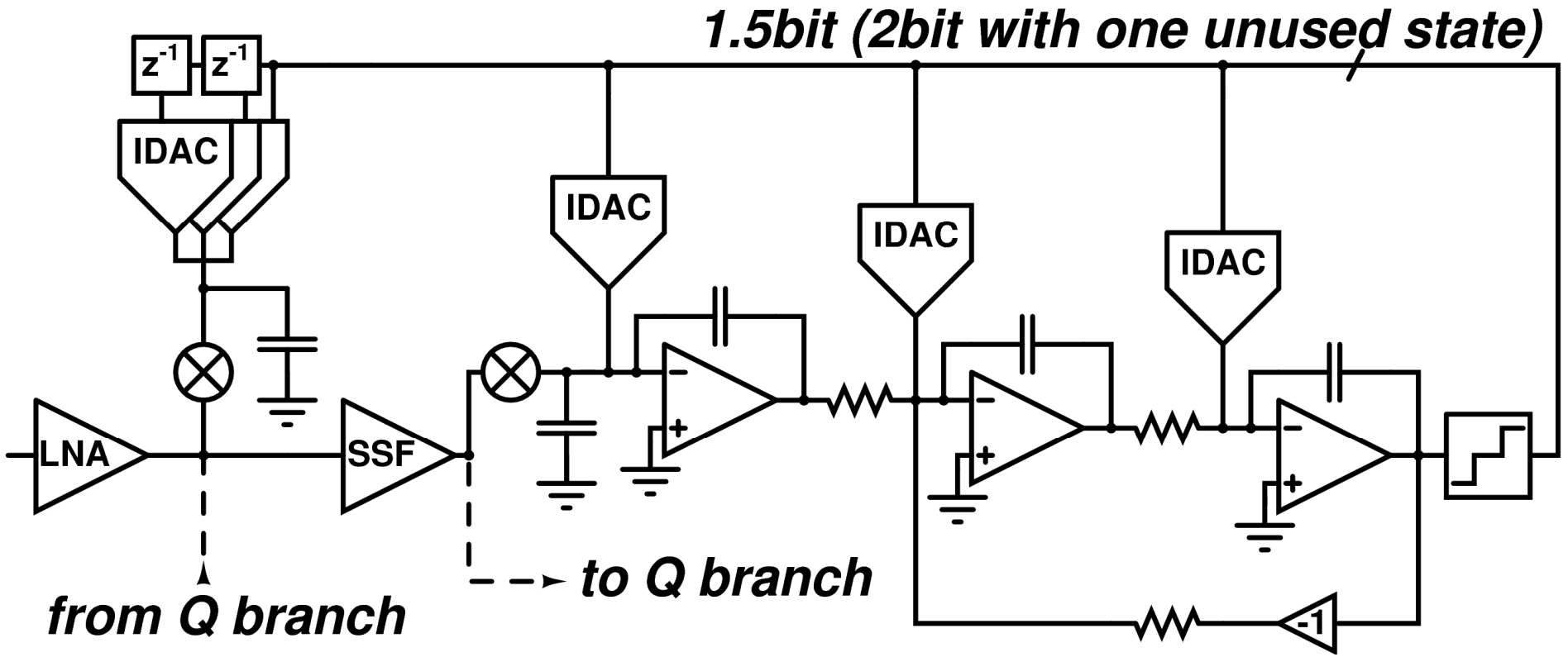
General DDSR Overview

Signal Flow Graph of Implemented Circuit



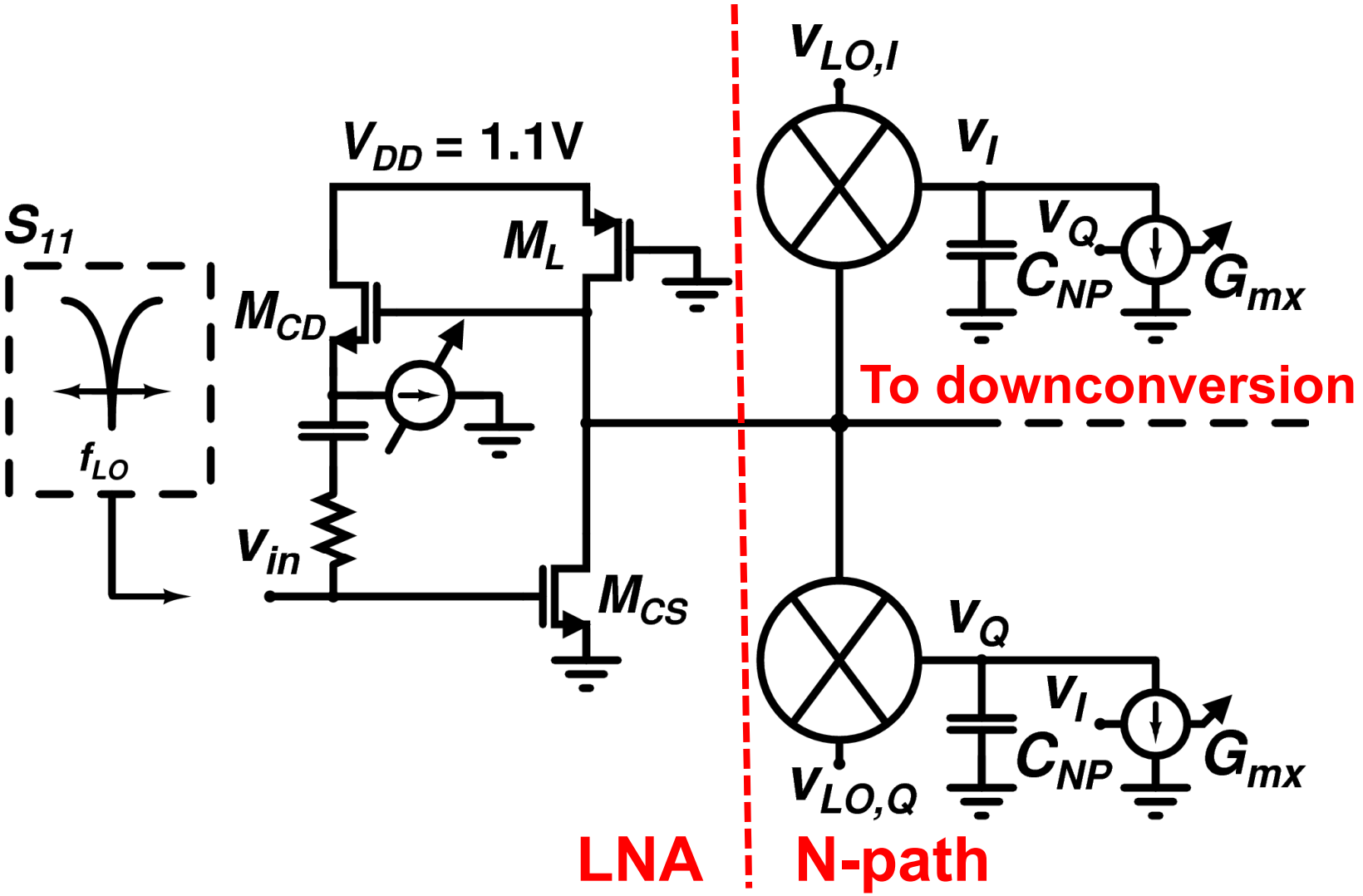
General DDSR Overview

Block Diagram of Implemented Circuit



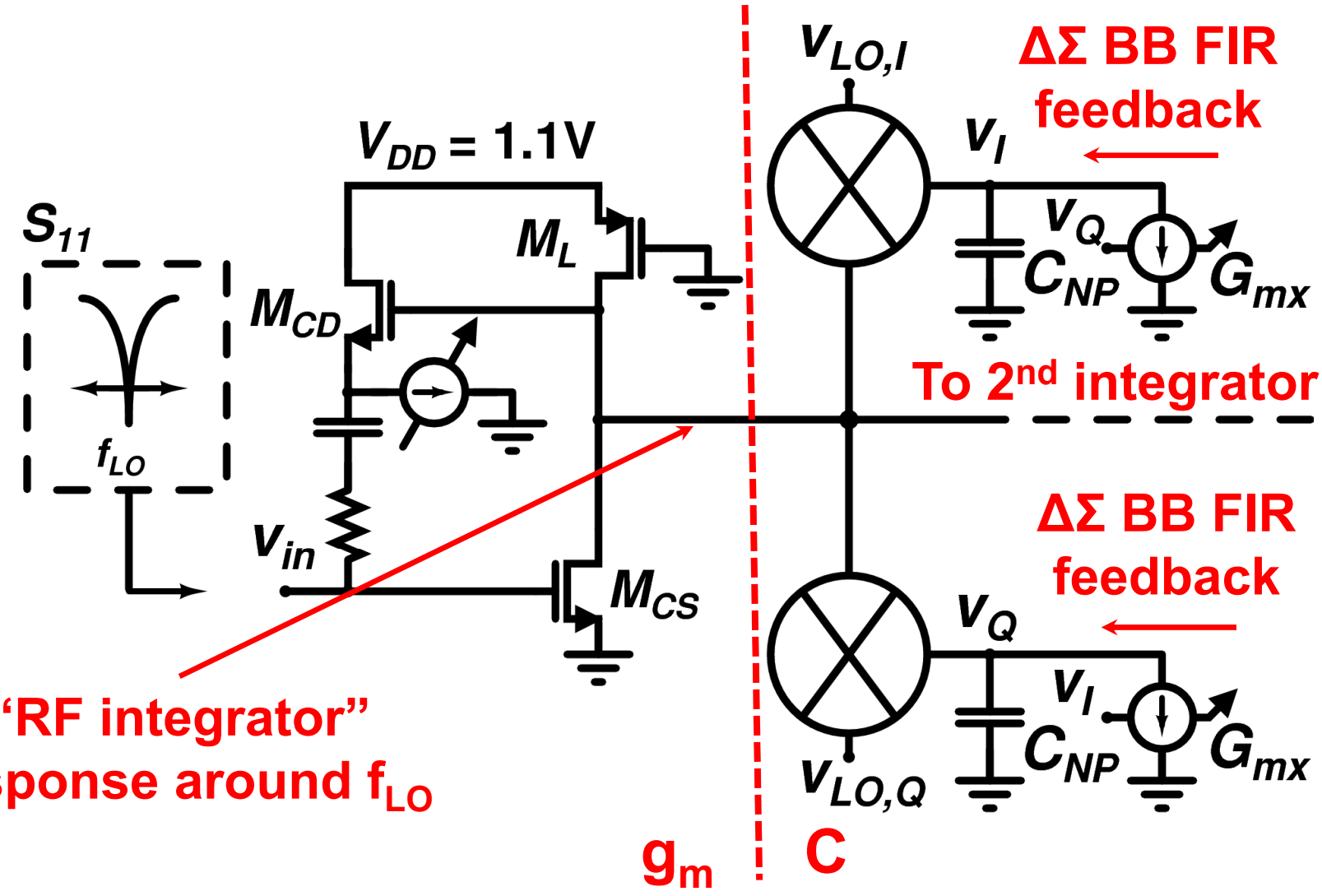
RF Section

First Integrator



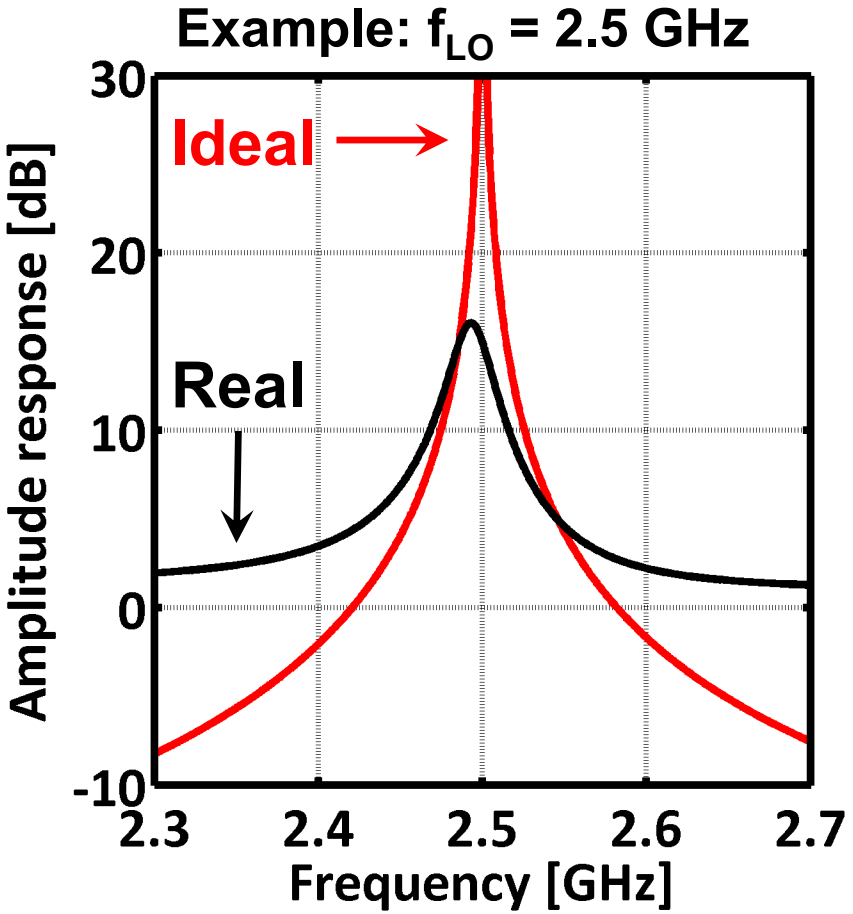
RF Section

First Integrator



RF Section

First Integrator – Main non-idealities

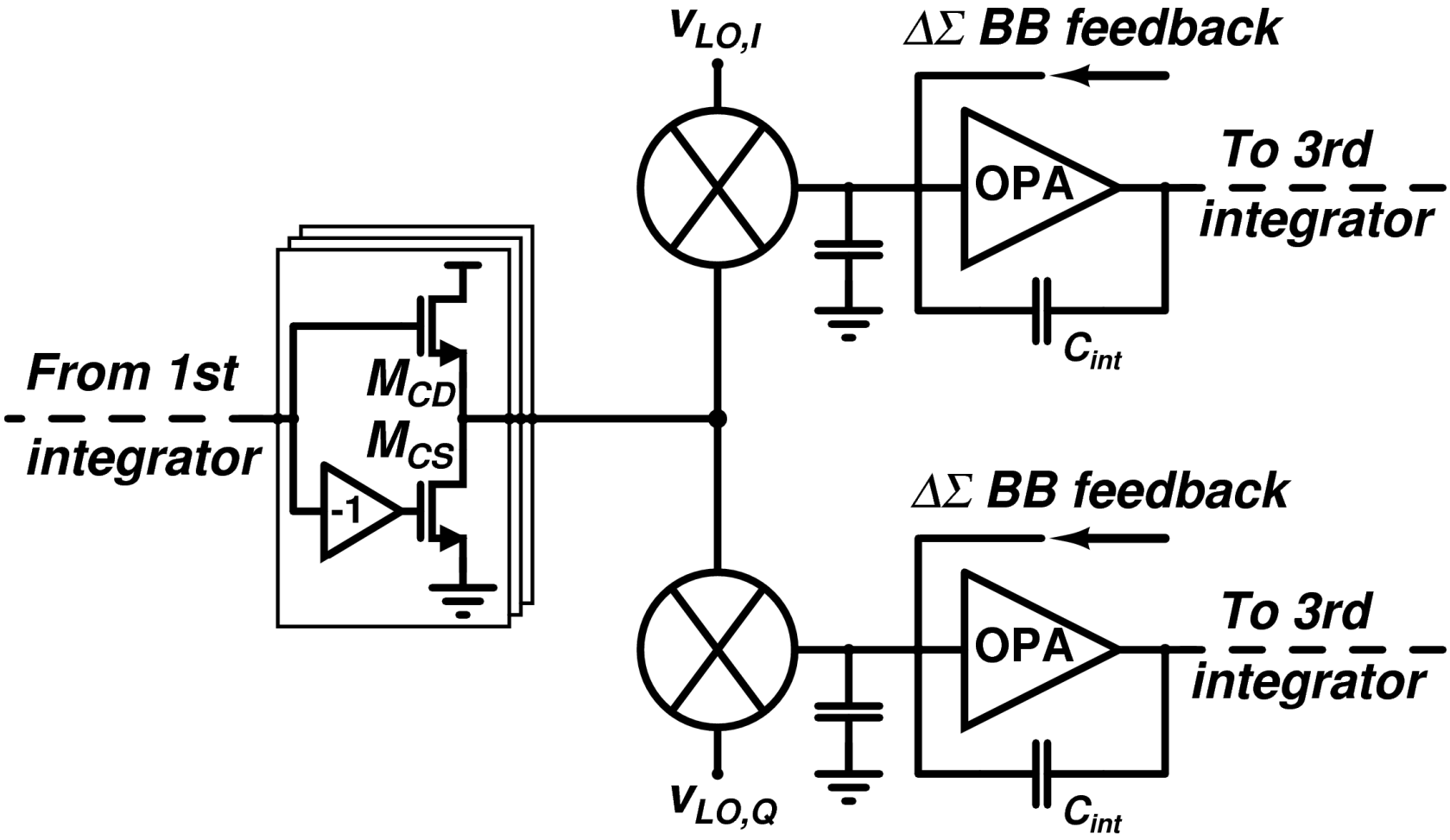


- **Low transcond. Z_{out}**
  - ⇒ Low "DC" (i.e., f_{LO}) gain
- **Presence of mixer R_{SW}**
  - ⇒ Limited OB attenuation
- **Center frequency shift**
  - ⇒ Sideband imbalance
- **N-path consequence**
  - ⇒ Periodic response
  - ⇒ Harmonic folding

Östman et al., *TCAS-2 2014*

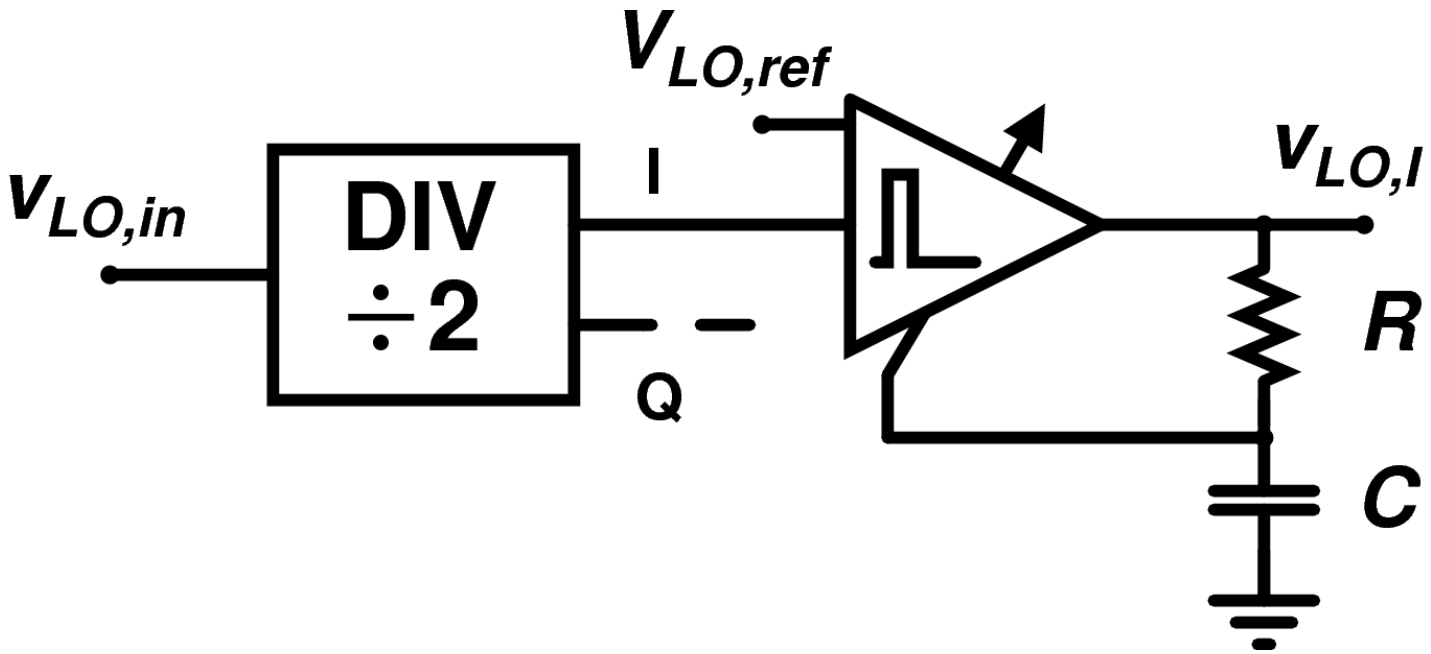
RF Section

Second Integrator "Downconverting g_mOPA-C integrator"



RF Section

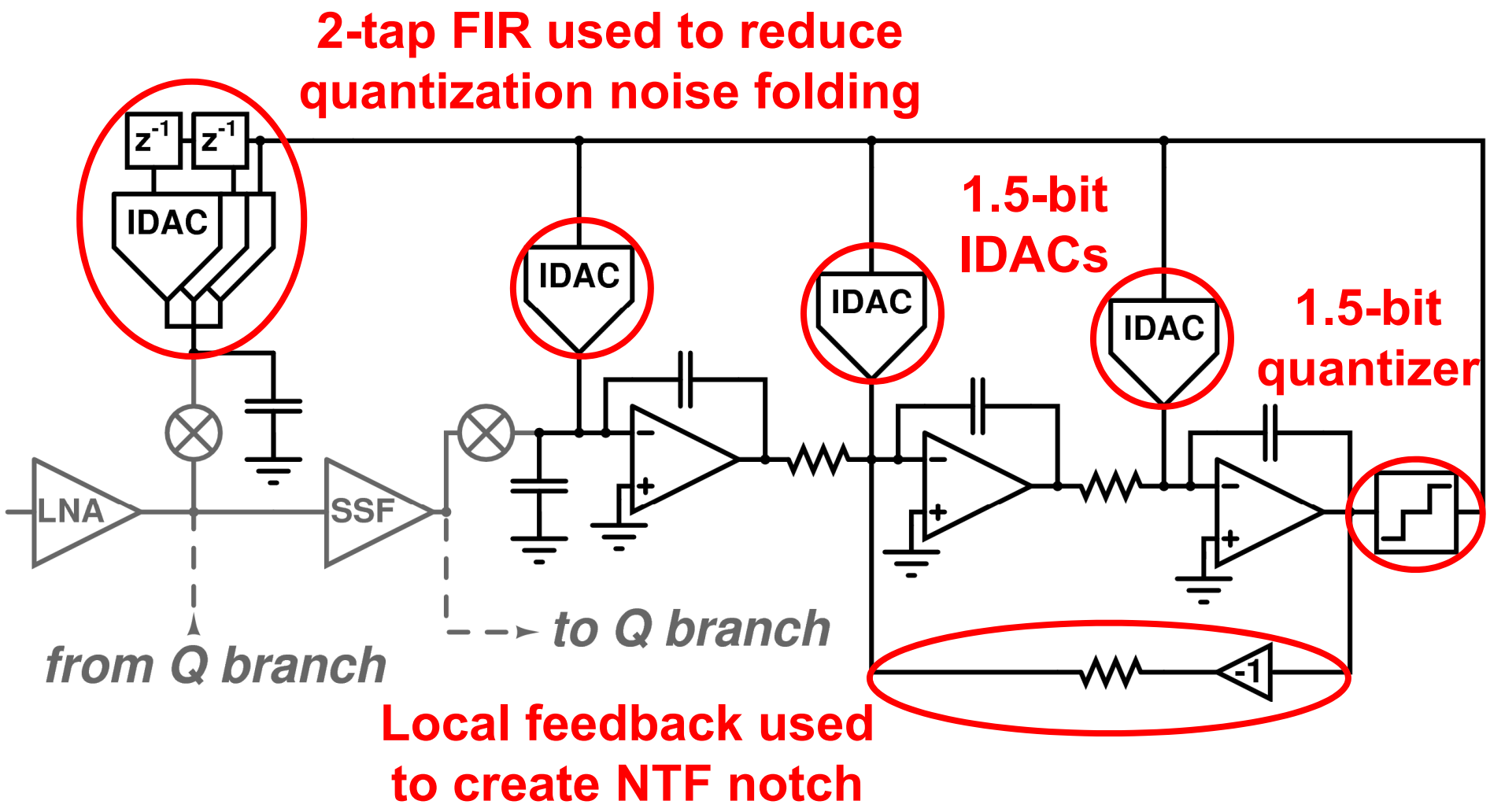
LO Buffering



- Separate final buffering for downconversion mixer and N-path filter

Baseband Section

General Structure

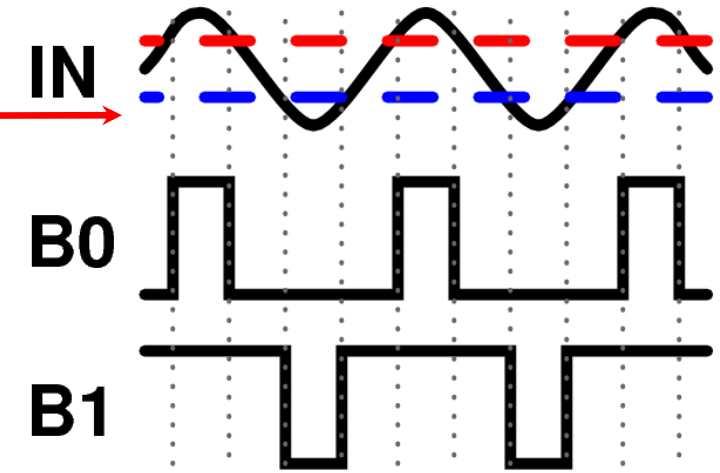


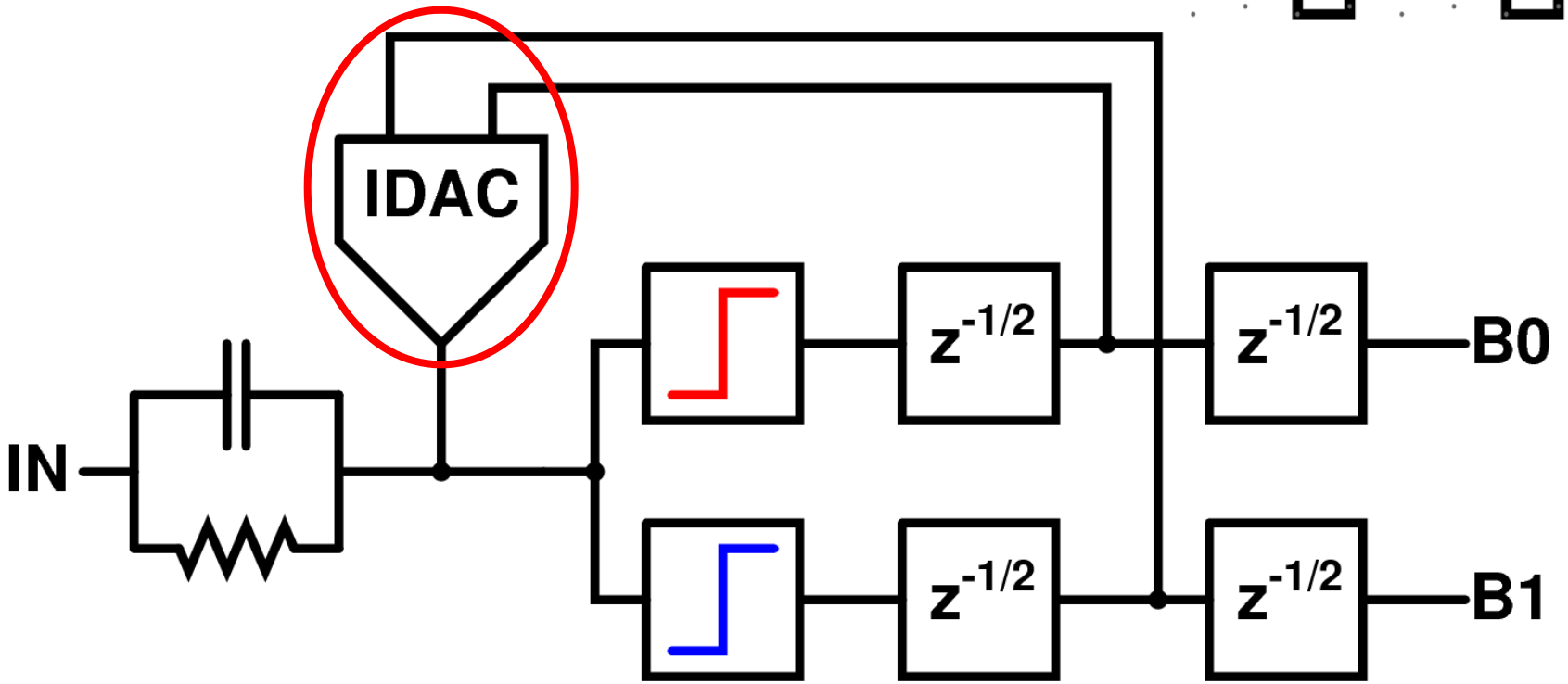
Baseband Section

1.5-bit Quantizer

Tunable references

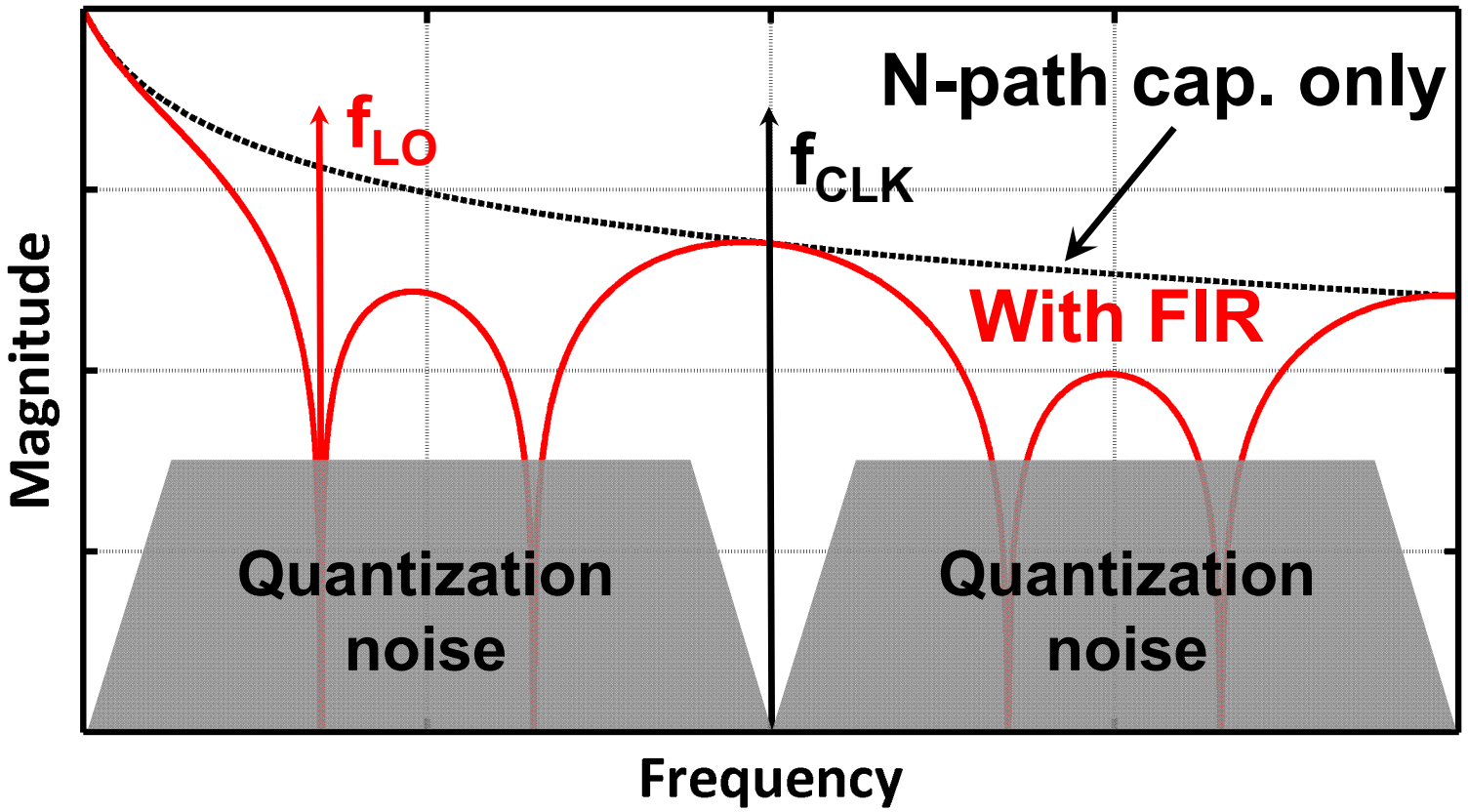
Excess loop delay compensation





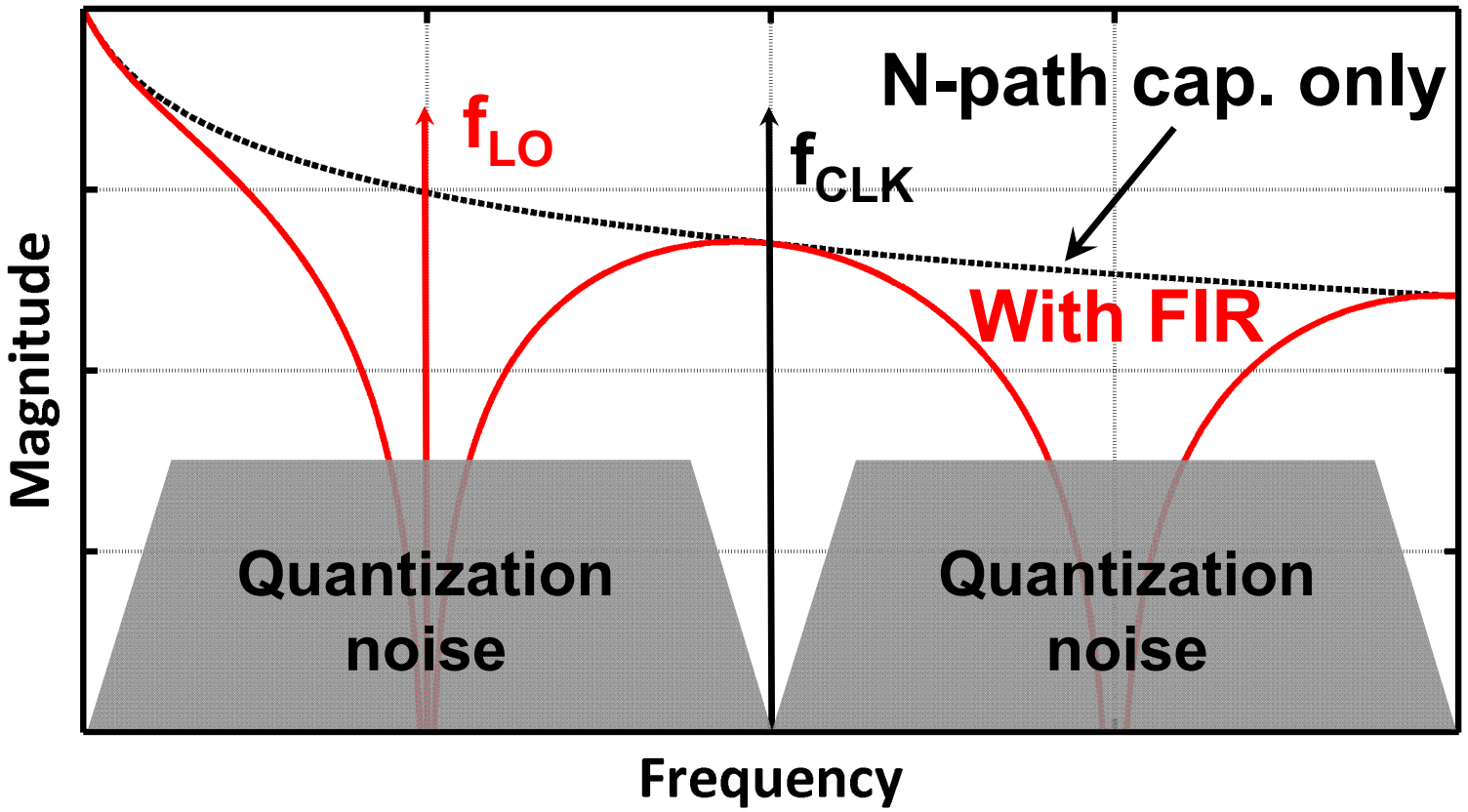
Baseband Section

1.5-bit 2-tap FIR and Minimal Noise Folding



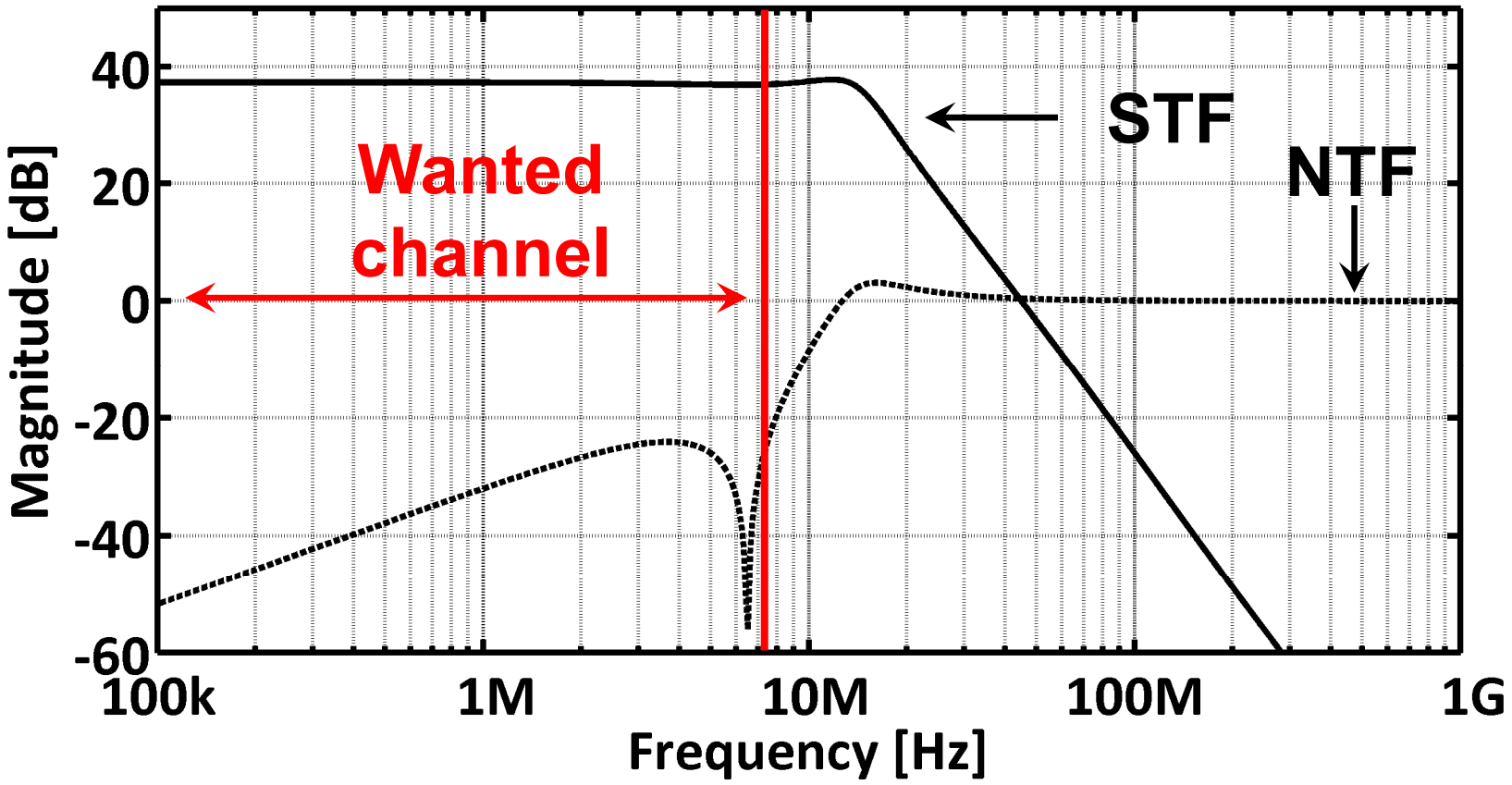
Baseband Section

1.5-bit 2-tap FIR and Minimal Noise Folding



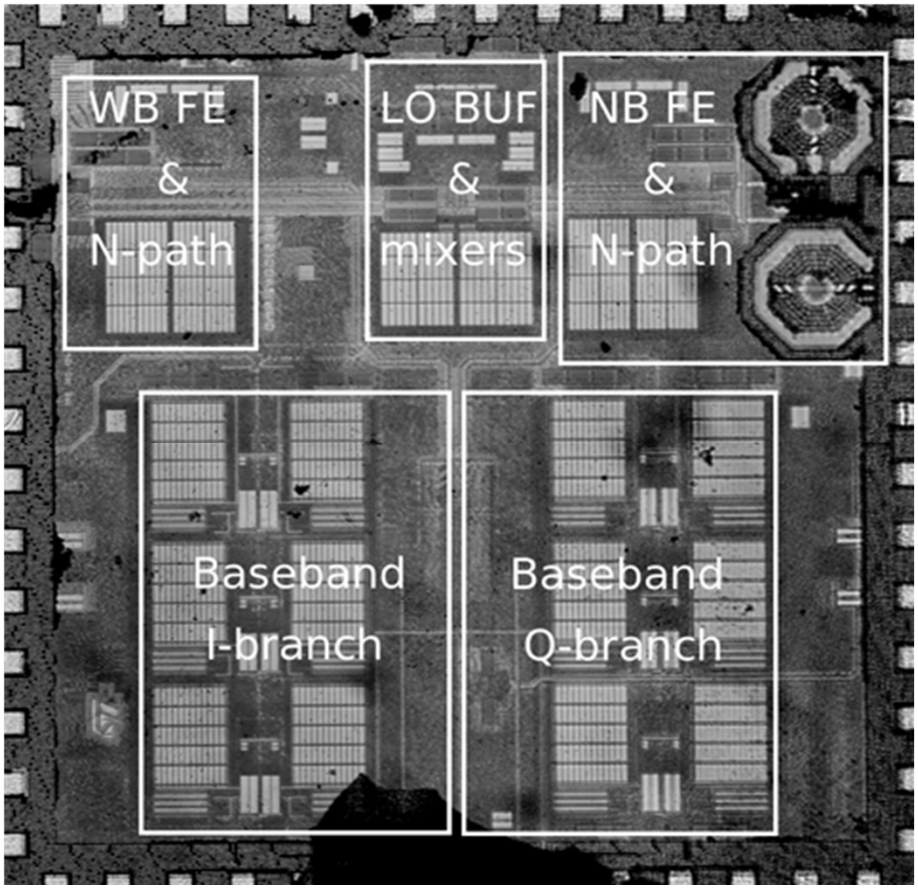
Baseband Section

NTF Notch



Experimental Results

Implementation

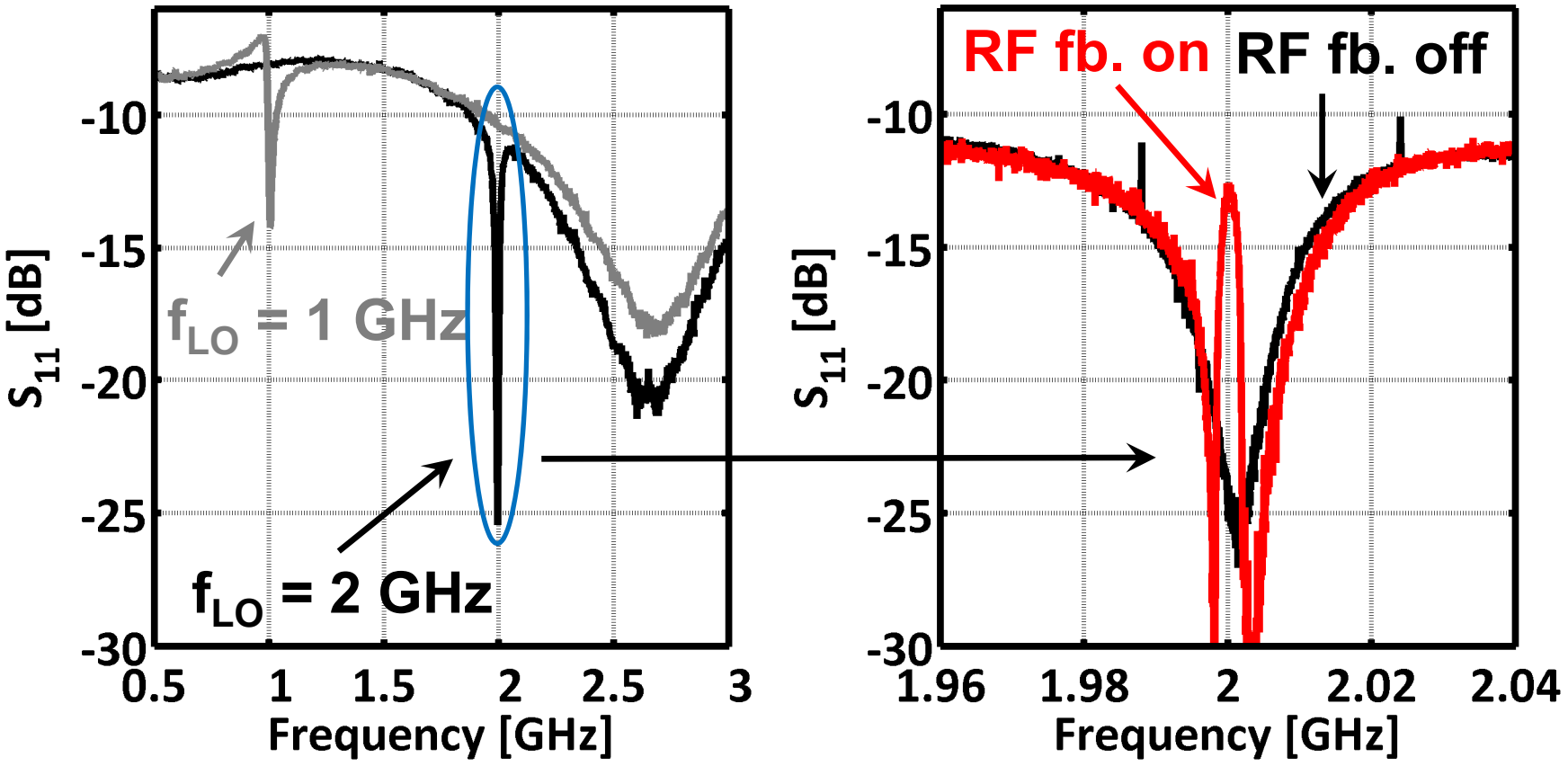


- 40-nm CMOS (1.1 V)
- Size 1.53 x 1.53 mm^2
- Packaged, 61-pin BGA

- Narrowband 2.5-GHz RX included as reference, shares the BB circuitry

Experimental Results

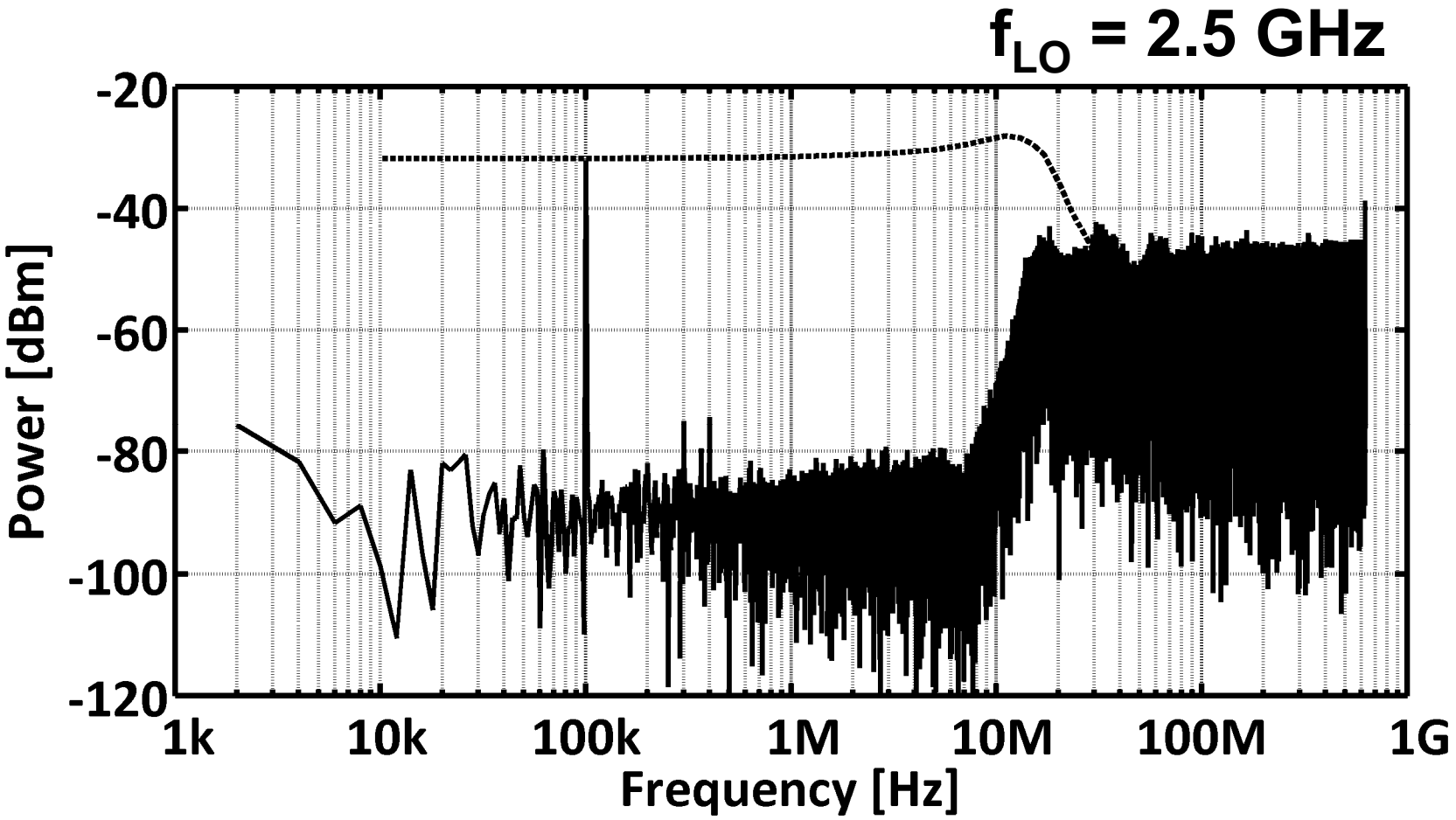
Input Matching



- RF feedback to LNA output affects in-band S_{11}

Experimental Results

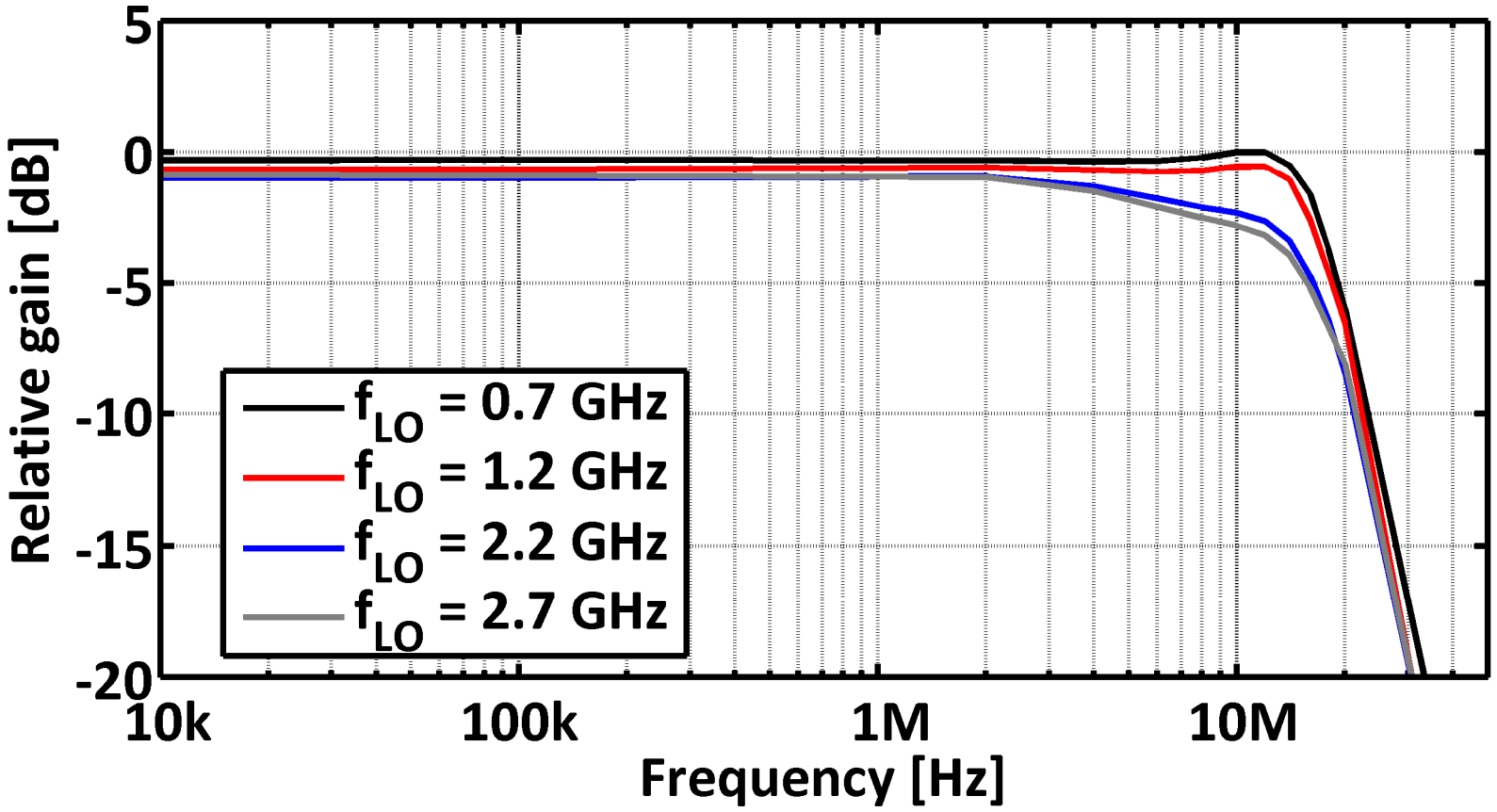
Output spectrum



- Efficient noise shaping easily leads to STF peaking

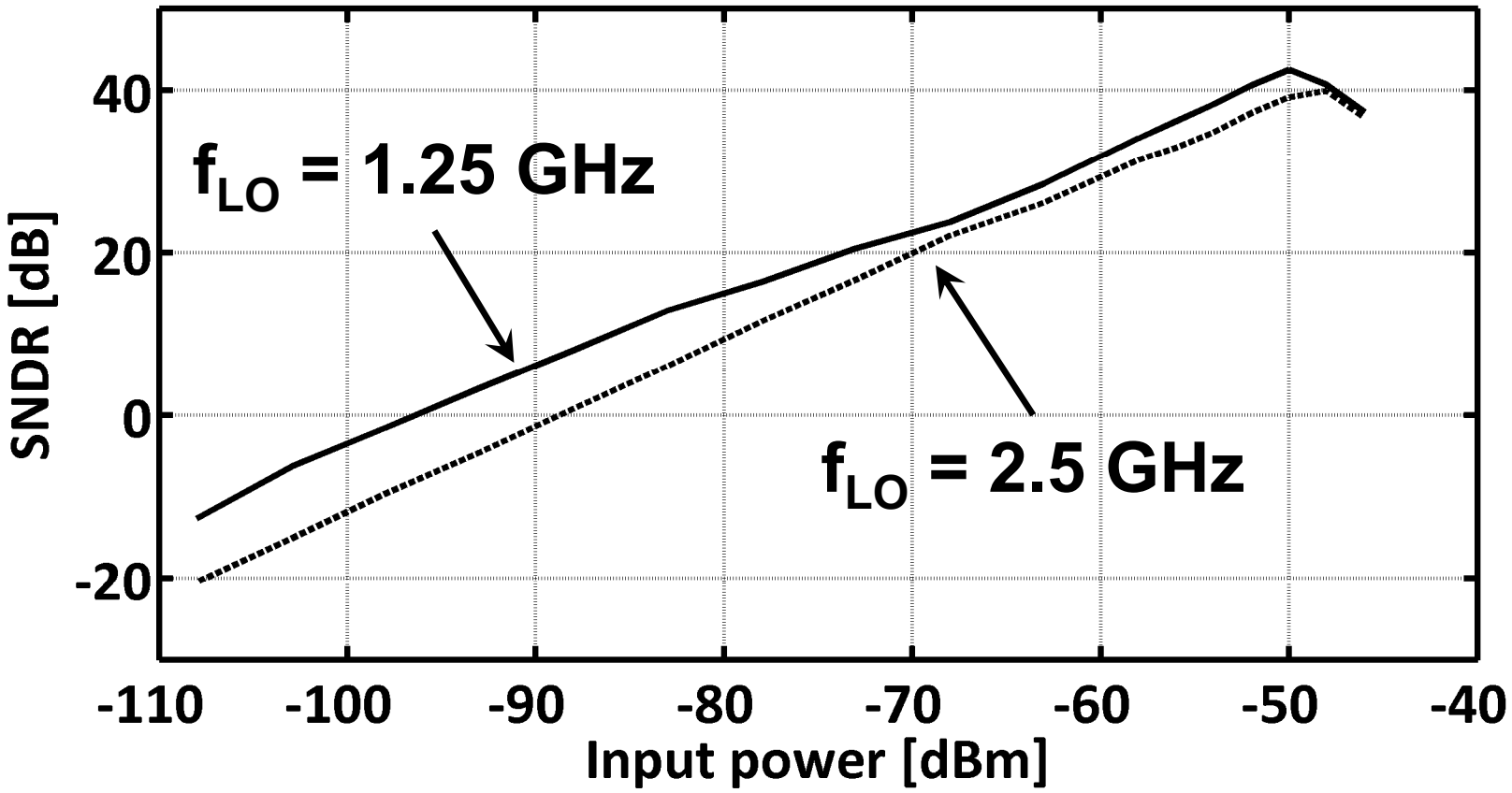
Experimental Results

STF vs. f_{LO}



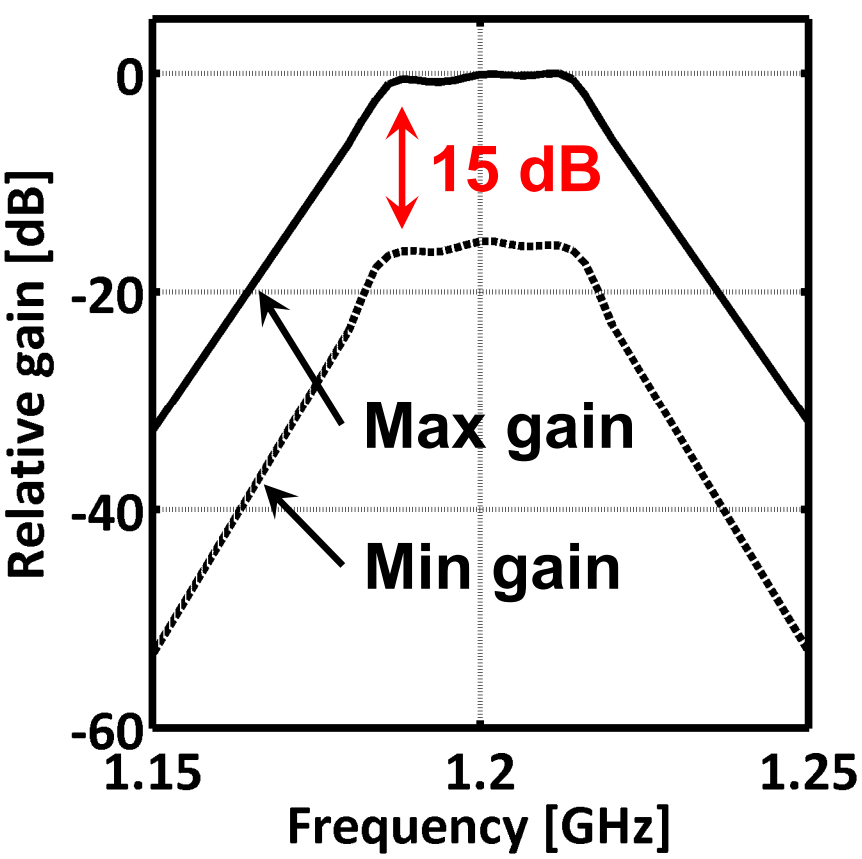
Experimental Results

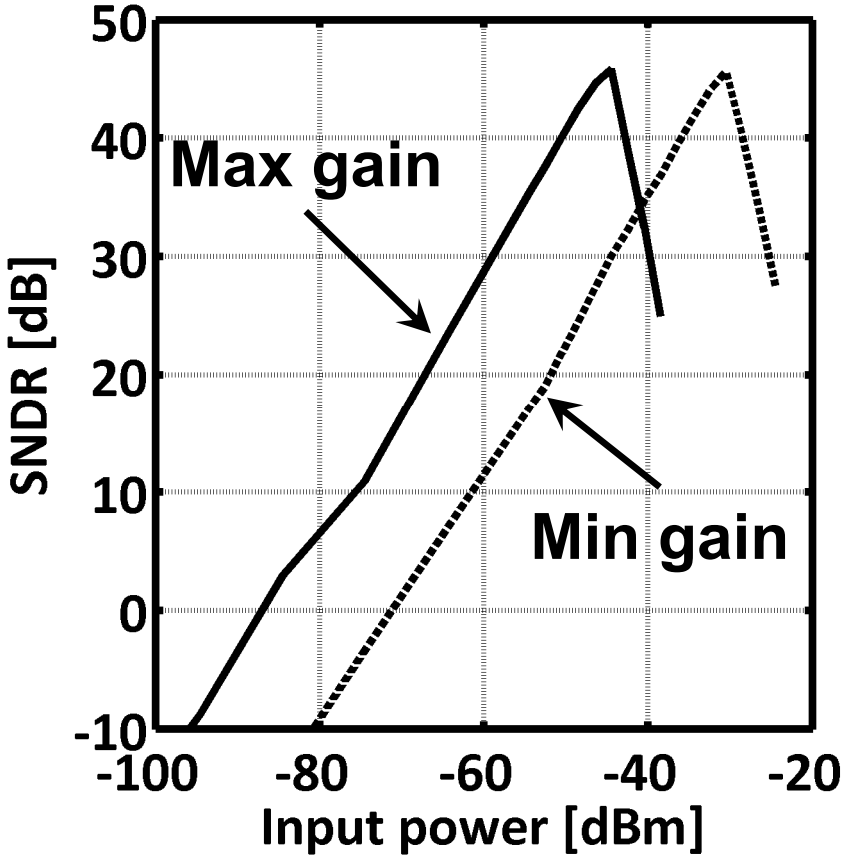
SNDR vs. P_{in}



Experimental Results

Gain Control

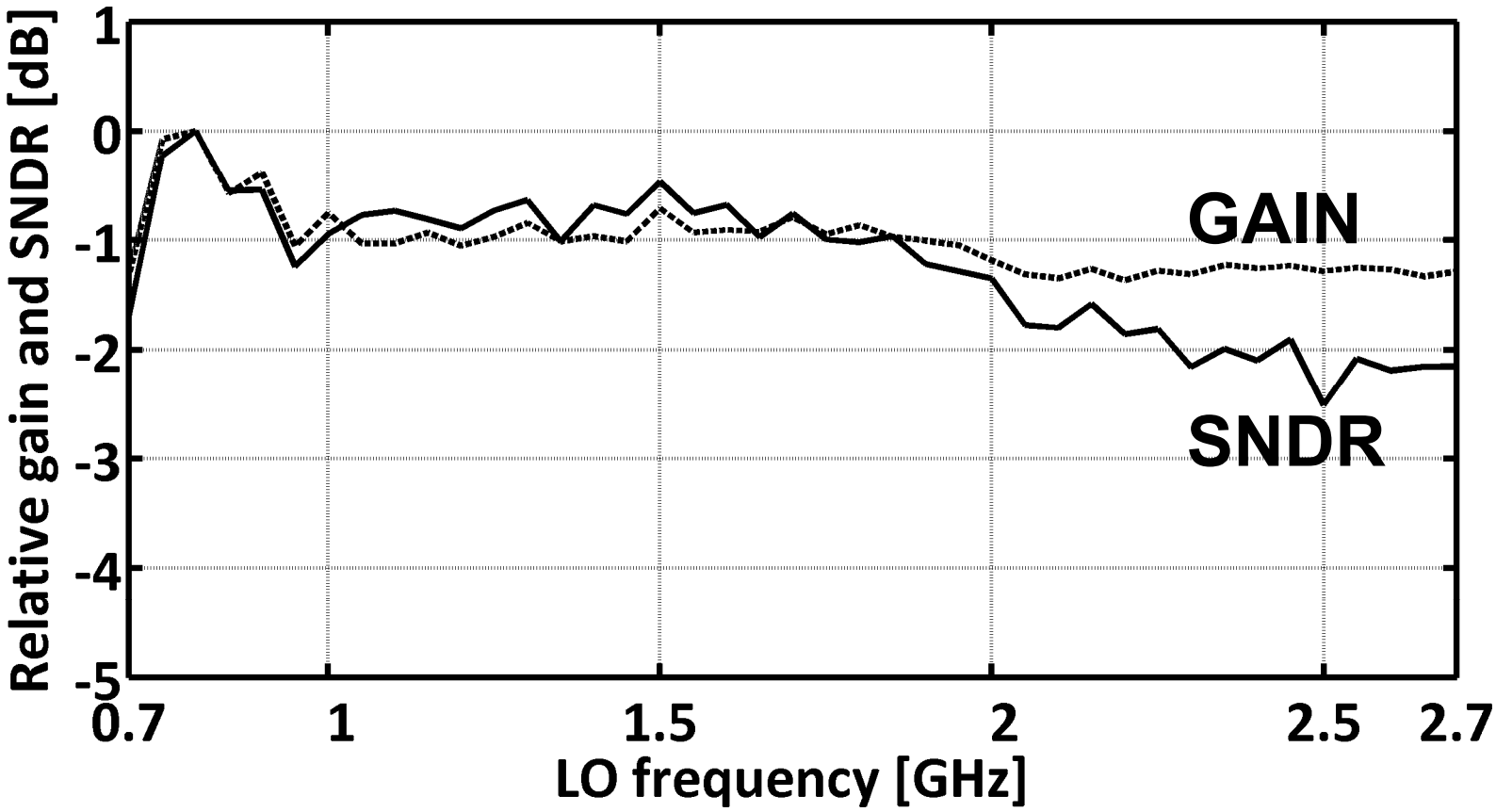




- STF shape retained by programming a_2 and b_1 in opposite directions

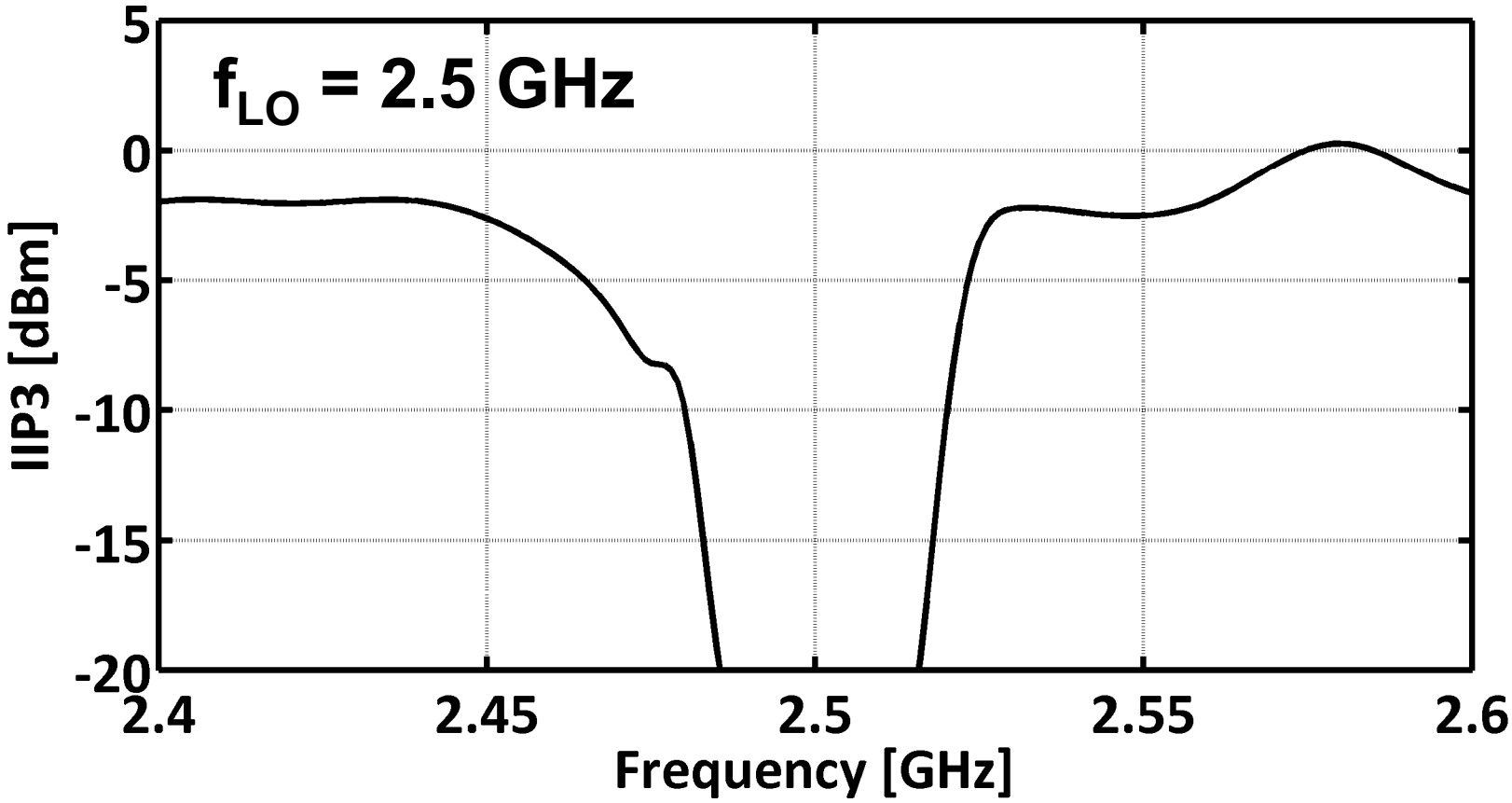
Experimental Results

Relative SNDR and Gain vs. f_{LO}



Experimental Results

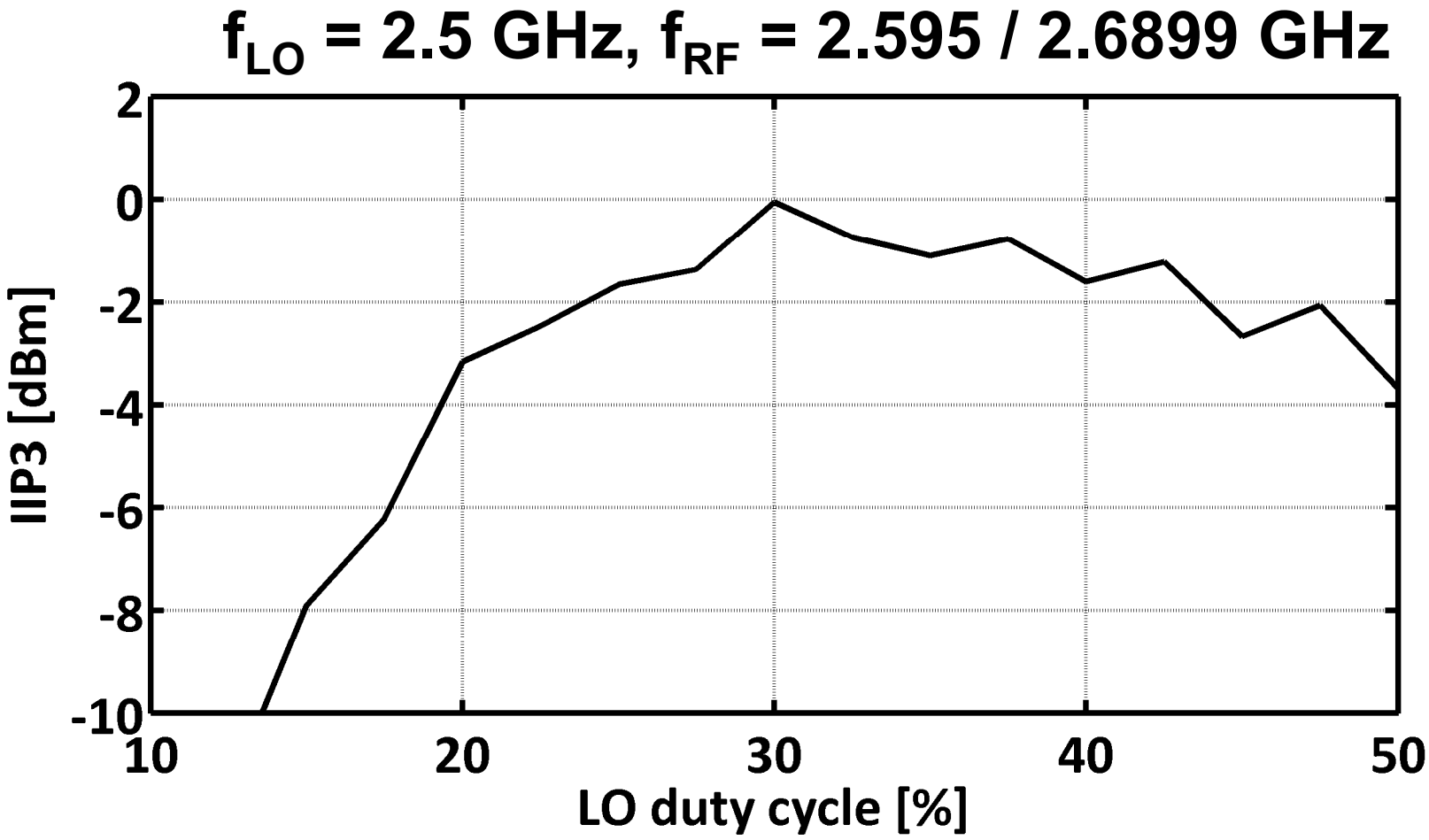
IIP3



- LNA limits OB IIP3 to about –2 dBm

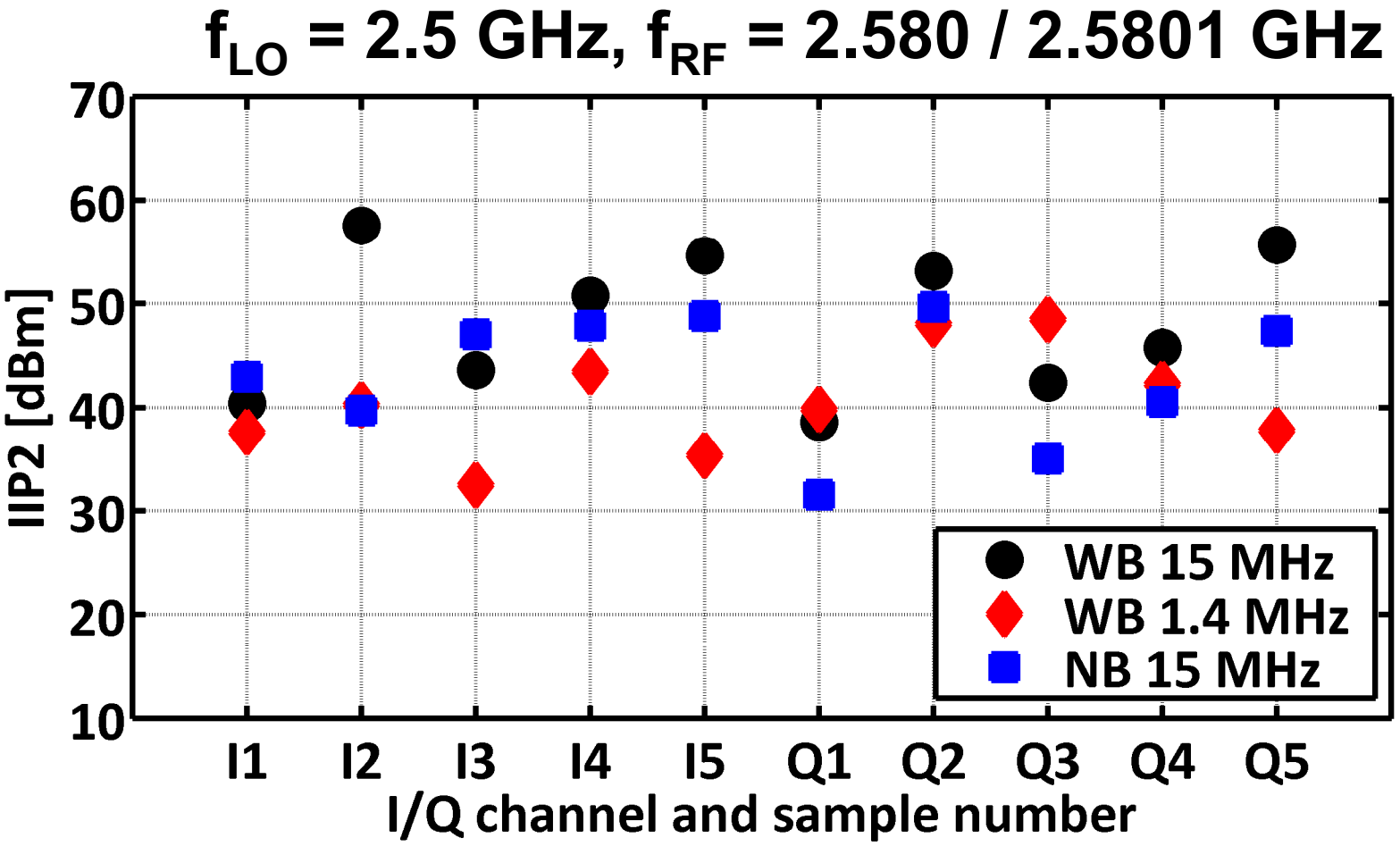
Experimental Results

IIP3



Experimental Results

IIP2



Experimental Results

Results Summary

Param. / RX Type	WB		NB (ref.)
LO Freq. [GHz]	0.7–2.7		2.5
Max CLK Freq. [GHz]	1.25		1
Sig. BW [MHz]	15	1.4	15
Gain [dB]	37	37	41
NF [dB]	5.9–8.8	5.9–8.2	4.2
OB IIP3 [dBm]	–2	–2	0
IIP2 [dBm]	>38	>35	>31
BCP–1dB [dBm]	–12	–14	–15
Max SNDR [dB]	43 (46)	40	50
Power [mW]	90@1.1V		

Conclusions

- The first active wideband DDSR
- Design philosophy targeted an optimum tradeoff between channel filtering and noise shaping
- Design methodology accounted for essential non-idealities in the RF stages
- Programmability in DSM coefficients and loop filter bandwidth

A 0.29mm^2 Frequency Synthesizer in 40nm CMOS with 0.19ps$_{rms}$ Jitter and <-100dBc Reference Spur for 802.11ac

Yu-Li Hsueh, Lan-Chou Cho, Chih-Hsien Shen,
Yi-Chien Tsai, Tzu-Chan Chueh, Tao-Yao Chang,
Jui-Lin Hsu, Jing-Hong Conan Zhan

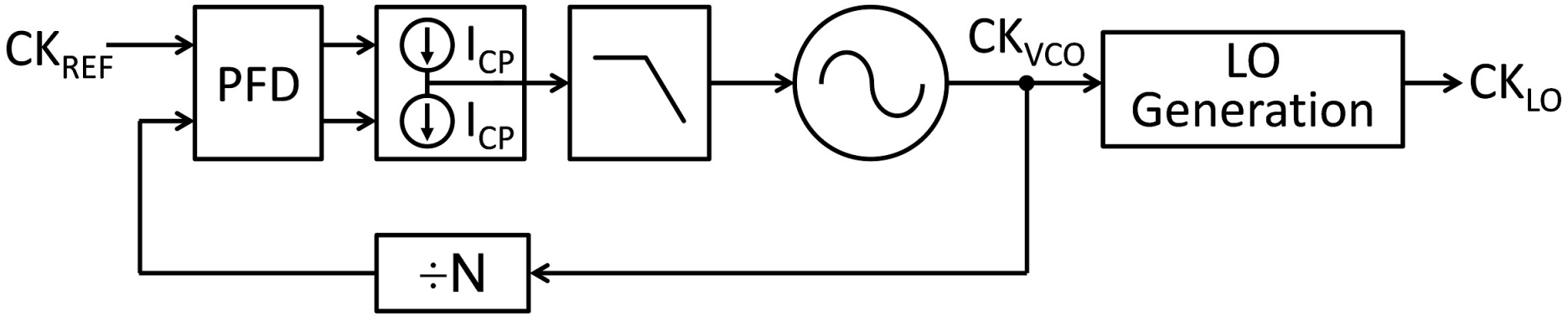
MediaTek, HsinChu, Taiwan

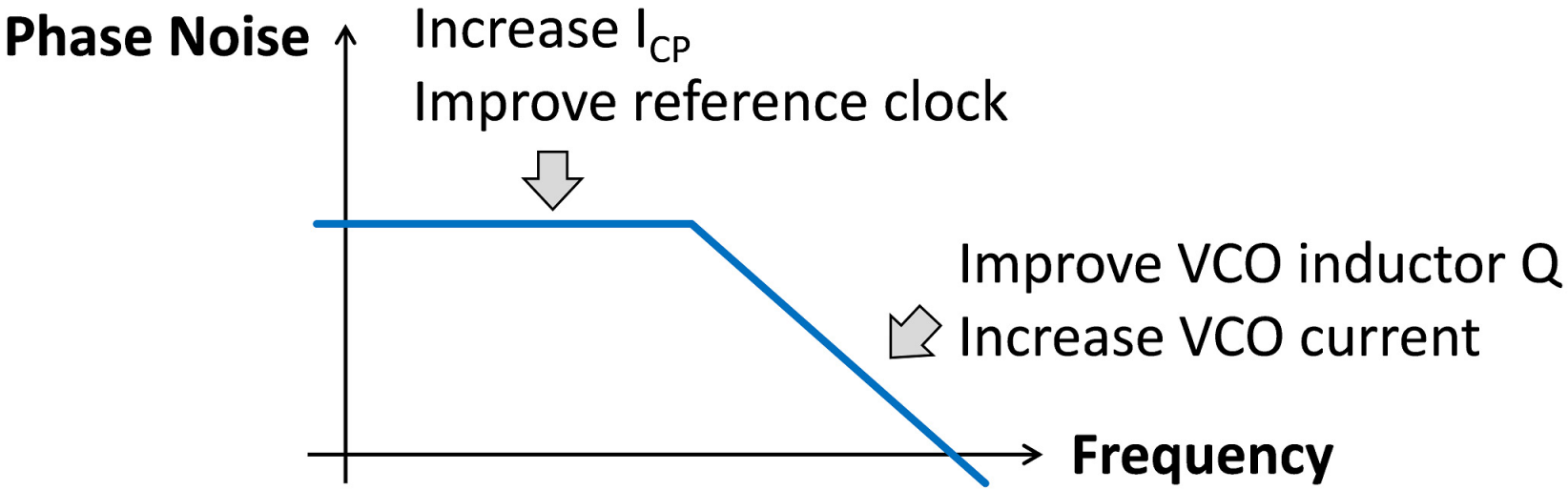
Paper 28.2

Contents

- Introduction
- Area-efficient **charge pump**
- Area re-used **loop filter**
- Reconfigurable **VCO** with improved biasing
- Inductor-less **2.4GHz LO generation**
- Compact **reference doubler**
- Measurement results
- Conclusion

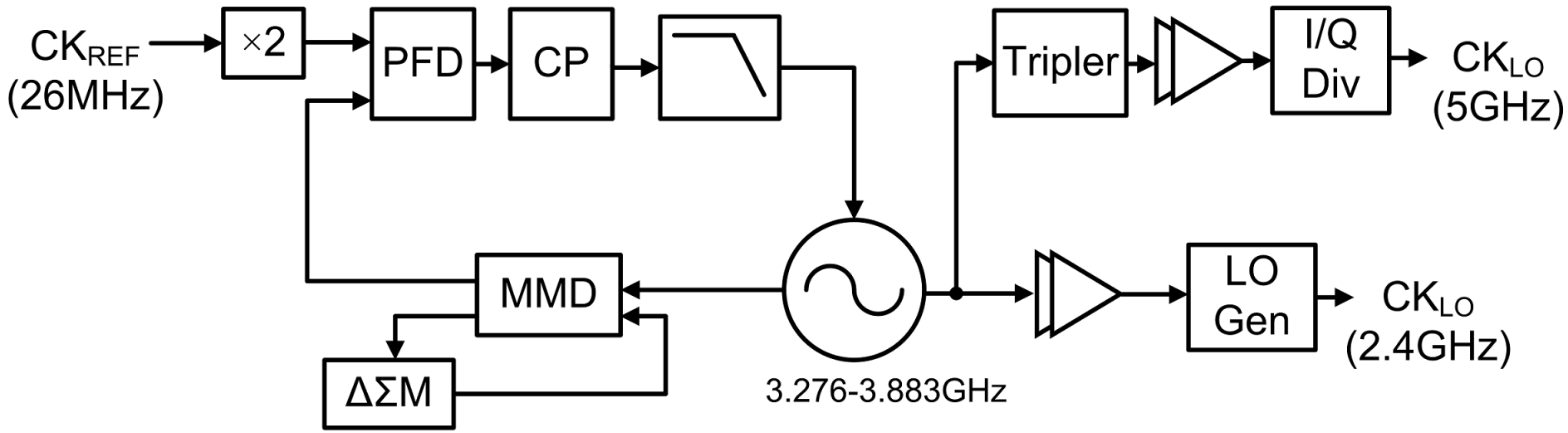
Frequency Synthesizer Phase Noise





Typically, **high-performance** requires **large area** and **high power**.

Frequency Synthesizer



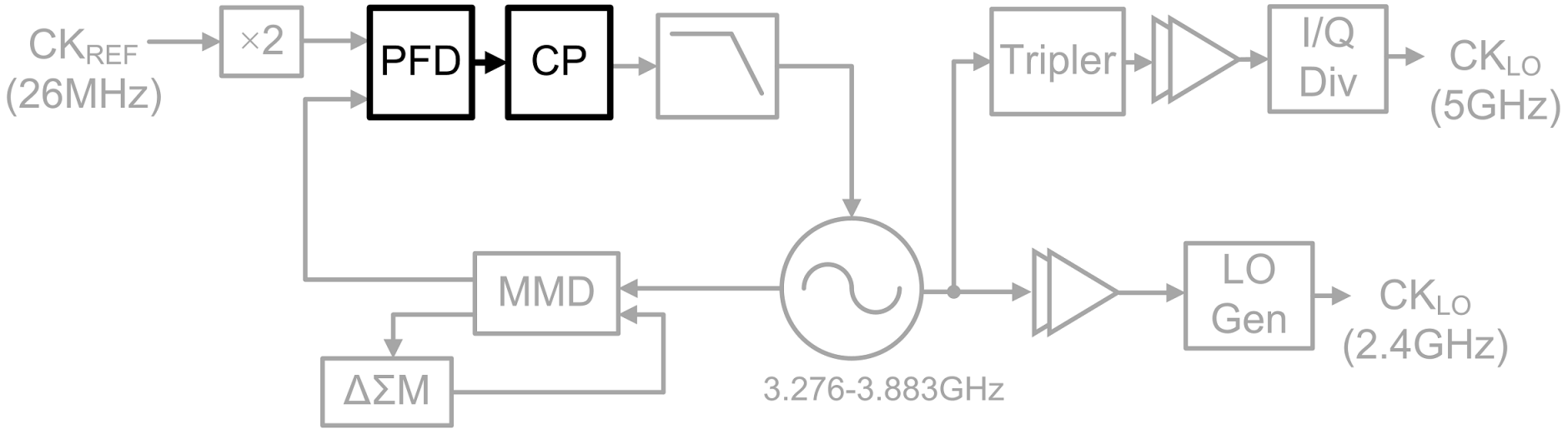
Jitter: 0.19ps$_{RMS}$ (F_{LO}=4915~5825MHz)

Reference Spur: <-100dBc (F_{REF}=26MHz)

FoM: -242dB (w/o ultra-thick metal, 40nm CMOS)

Area: 0.29mm^2

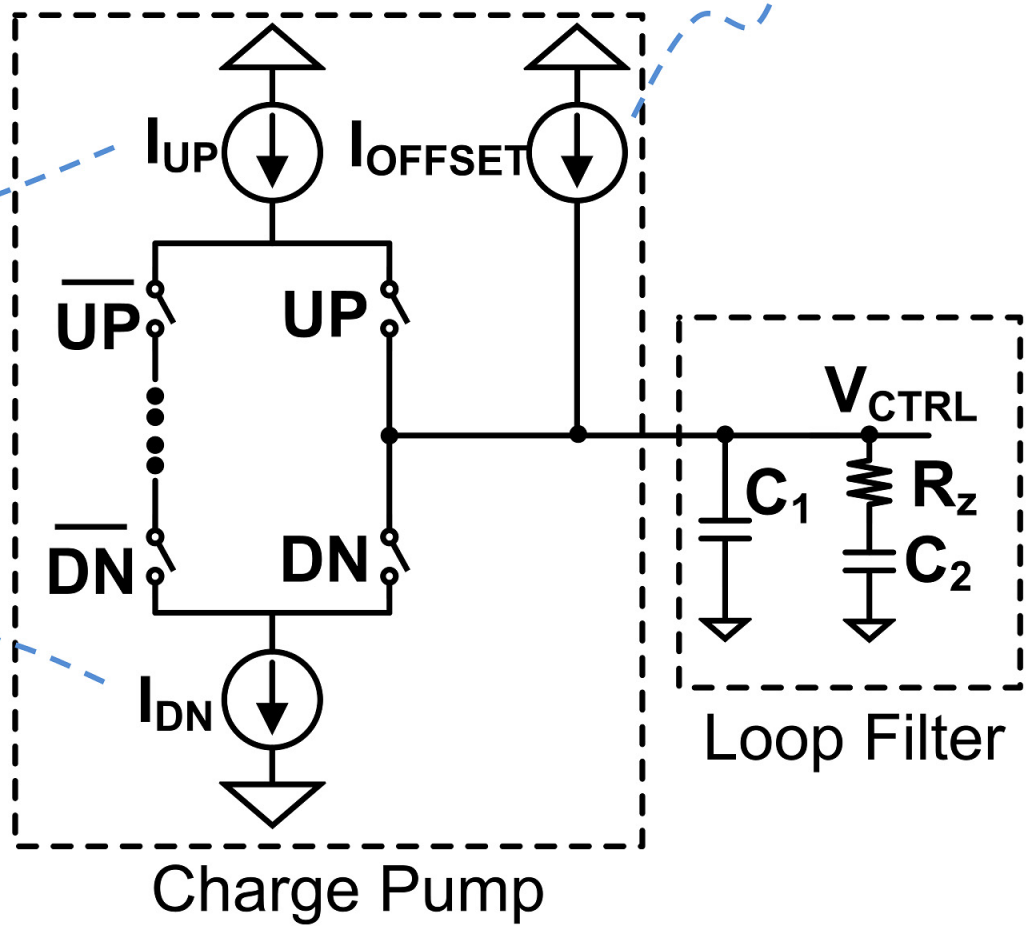
PFD and Charge Pump



Conventional Charge Pump

I_{OFFSET} shifts the operating point to avoid ΔΣM noise folding.

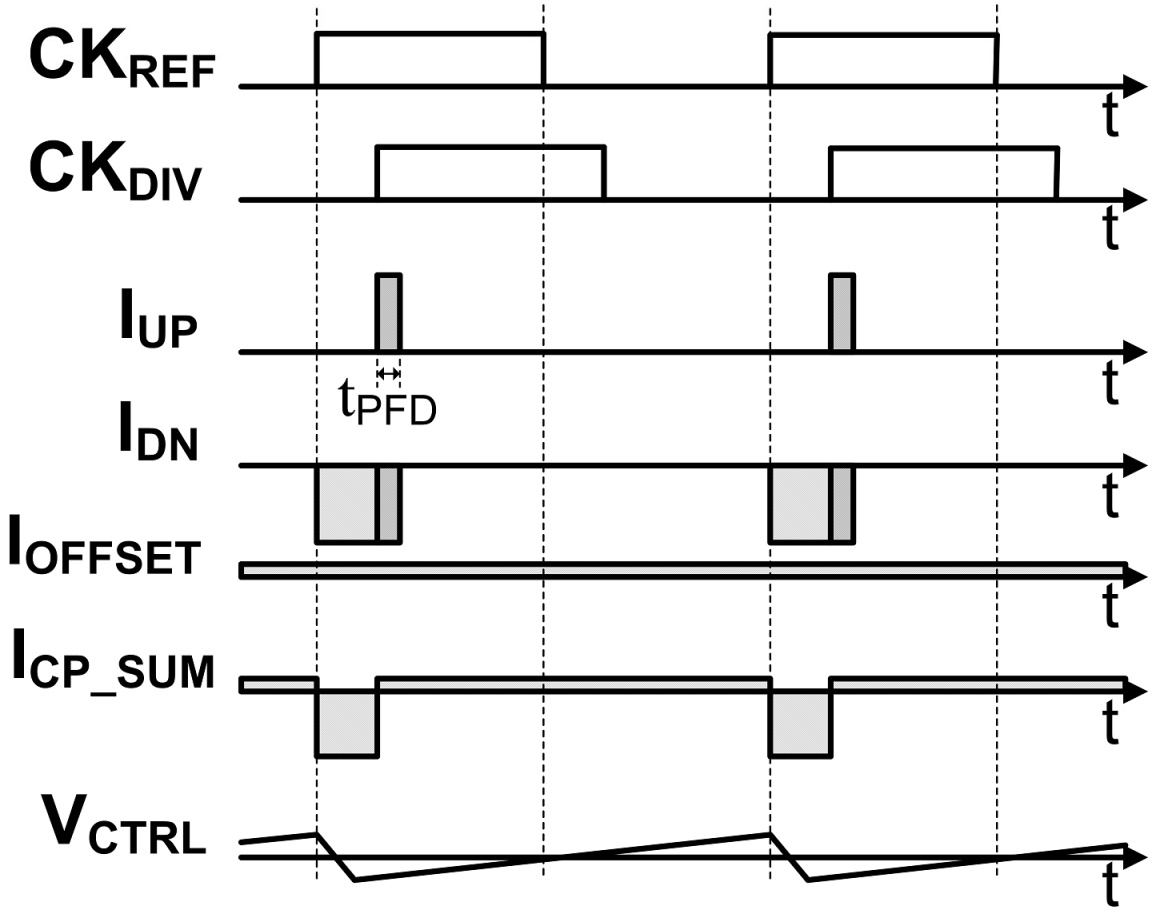
I_{UP} and I_{DN} occupy **large areas** for low noise & good matching.
Typical I_{UP} occupies >50% area.



Timing Diagram

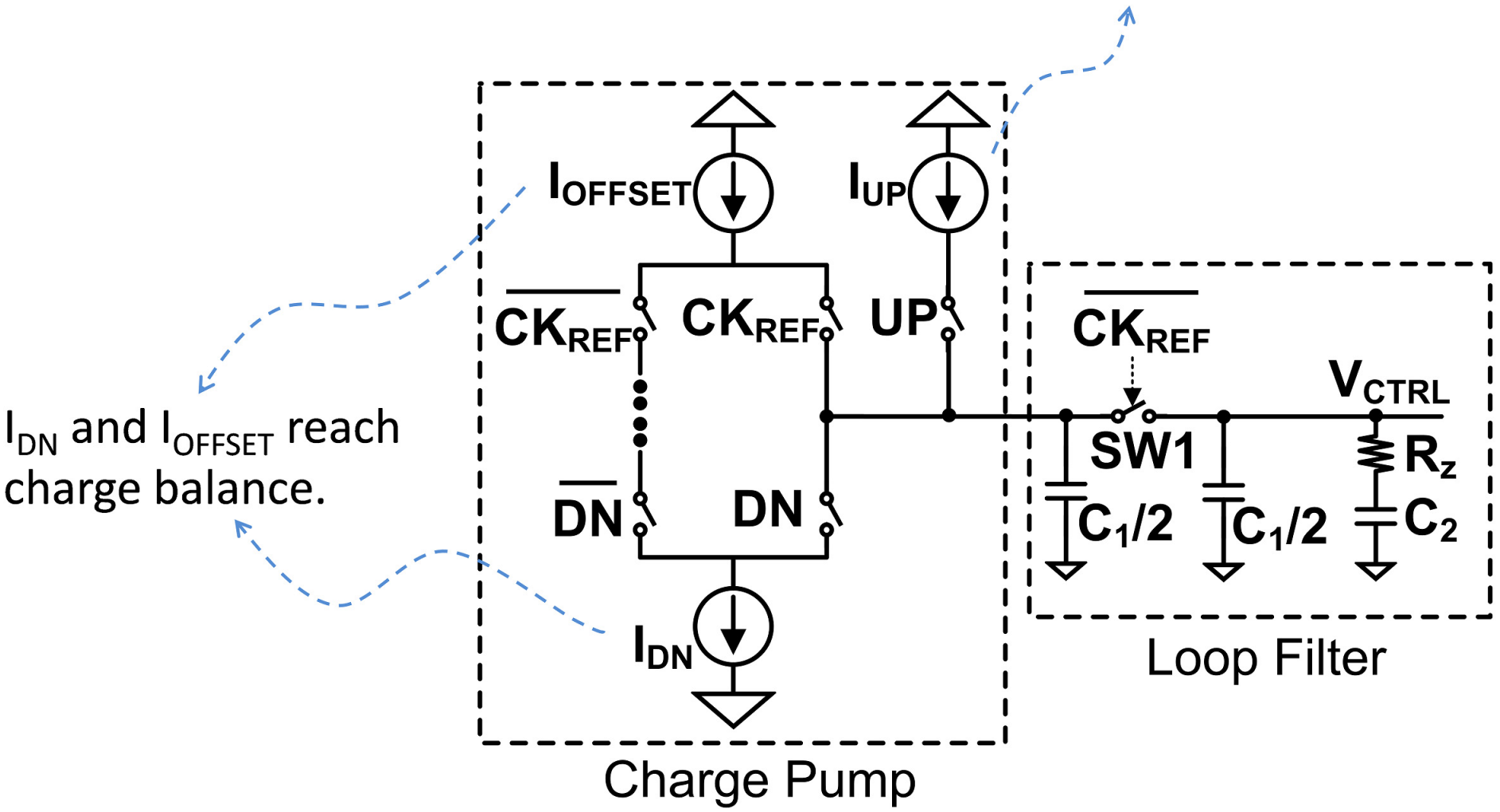
- I_{UP} exhibits a fixed length due to t_{PFD}

  ➔ I_{UP} and cancelled I_{DN} do nothing but add noises.



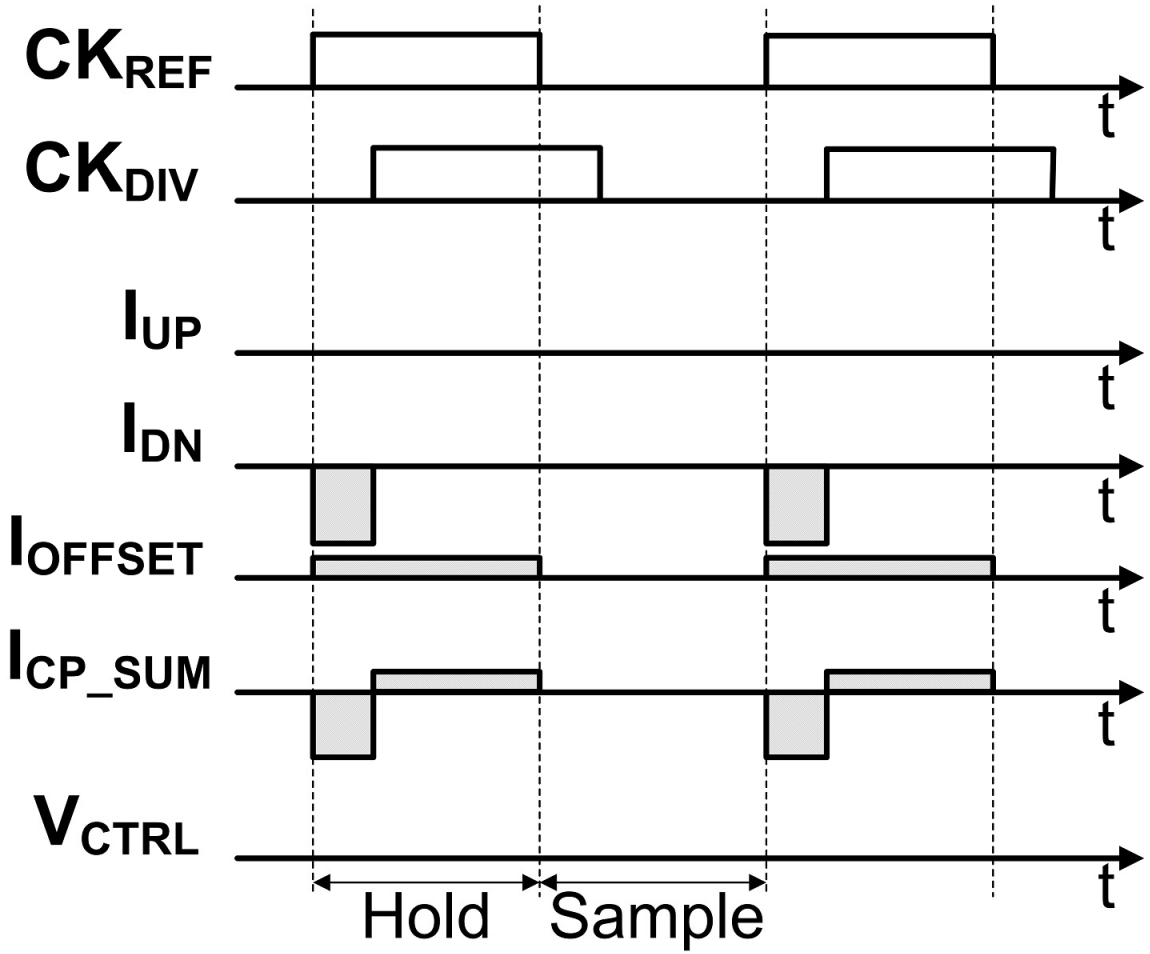
Proposed Charge Pump

I_{UP} is conditionally ON only when unlocked
➔ noise & matching are not important.

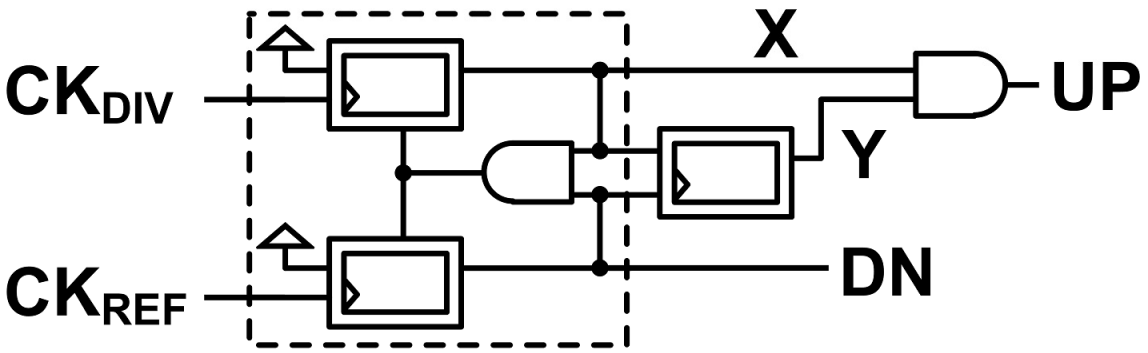


Timing Diagram

- I_{UP} is disabled → Relaxed design constraints.
- S&H using gated I_{OFFSET} reduces reference spur.

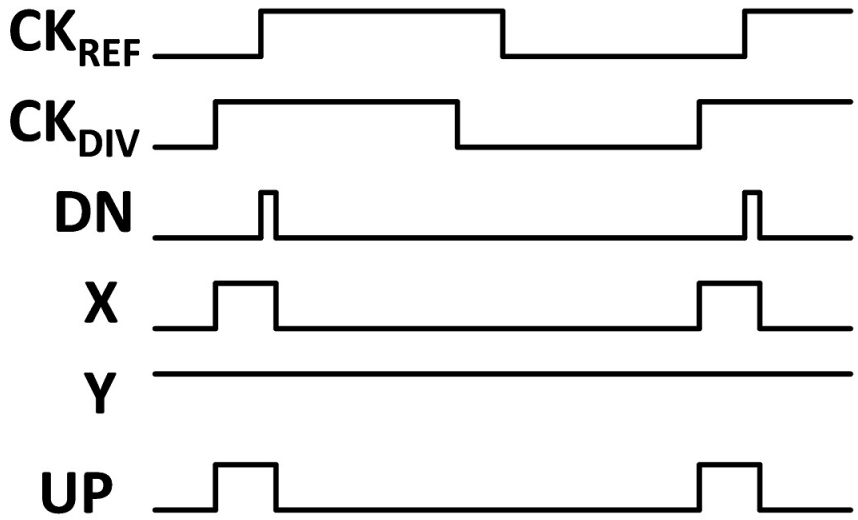


PFD

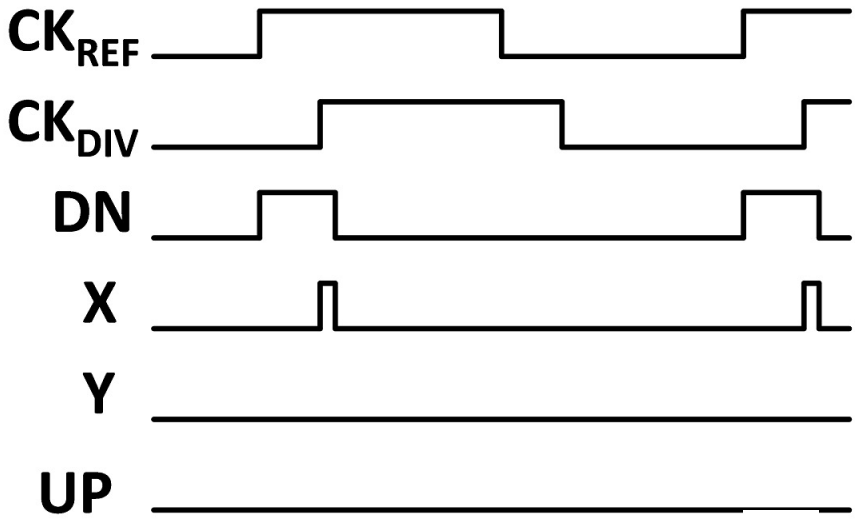


(Conventional PFD)

CK_{REF} lags CK_{DIV}

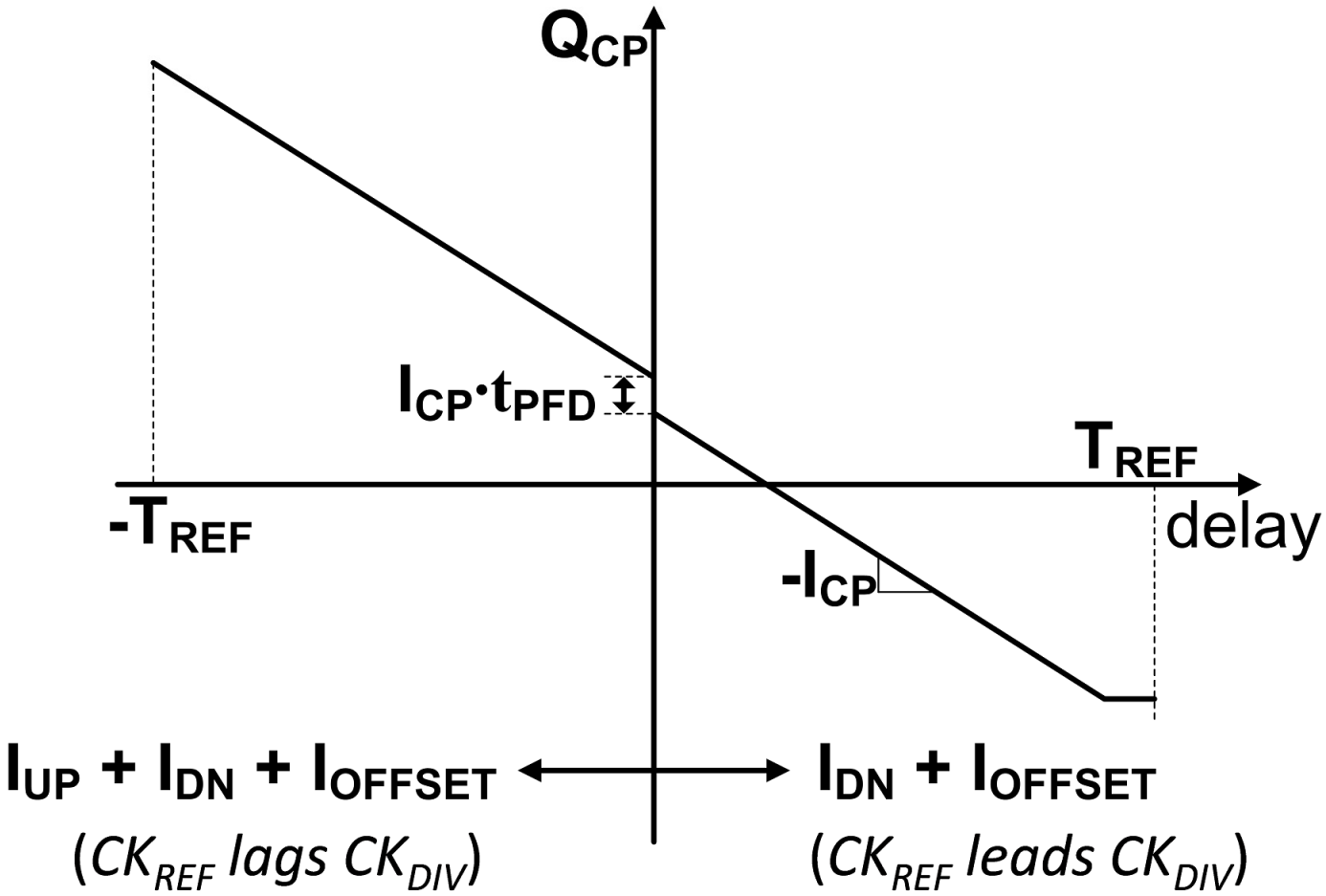


CK_{REF} leads CK_{DIV}

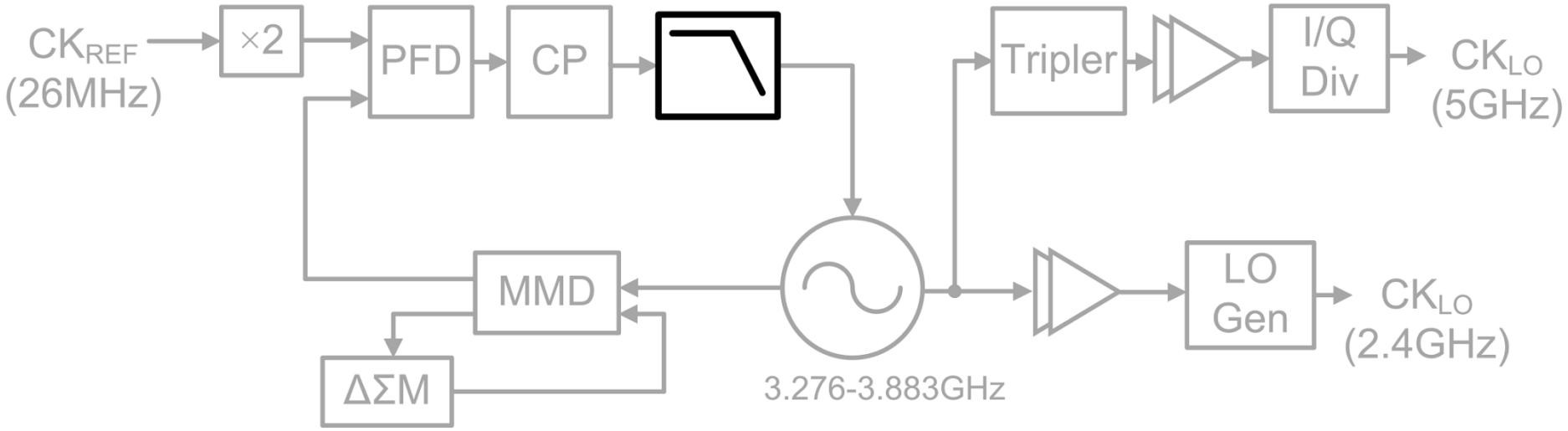


Q-vs-Delay Diagram

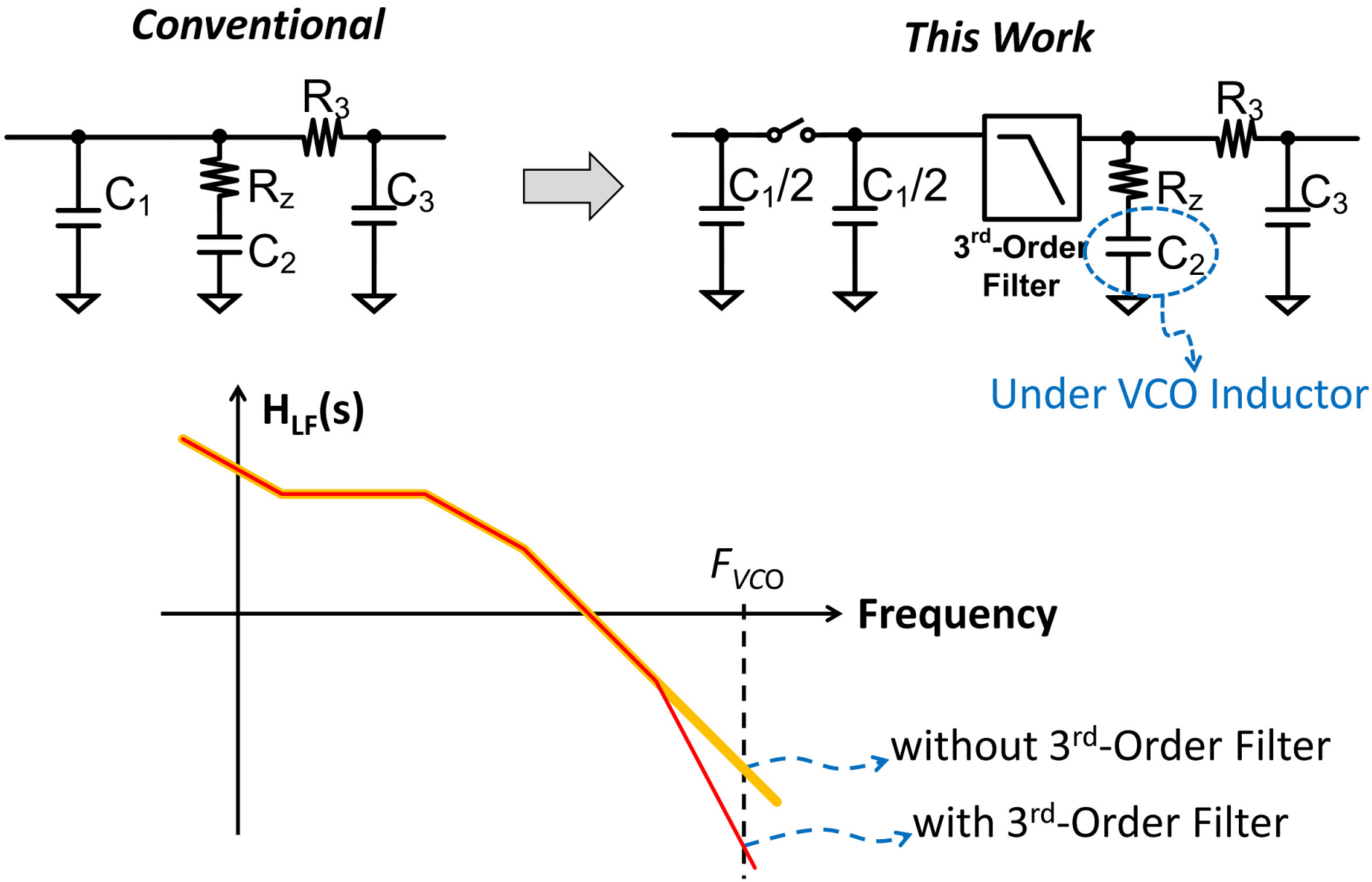
- When unlocked, I_{UP} is conditionally ON.
- When phase-locked, I_{DN} and I_{OFFSET} reach balance.



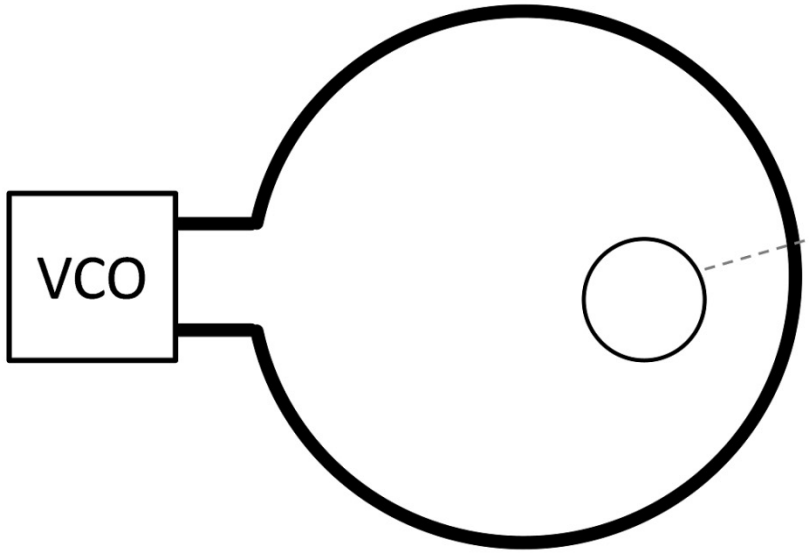
Loop Filter



Loop Filter

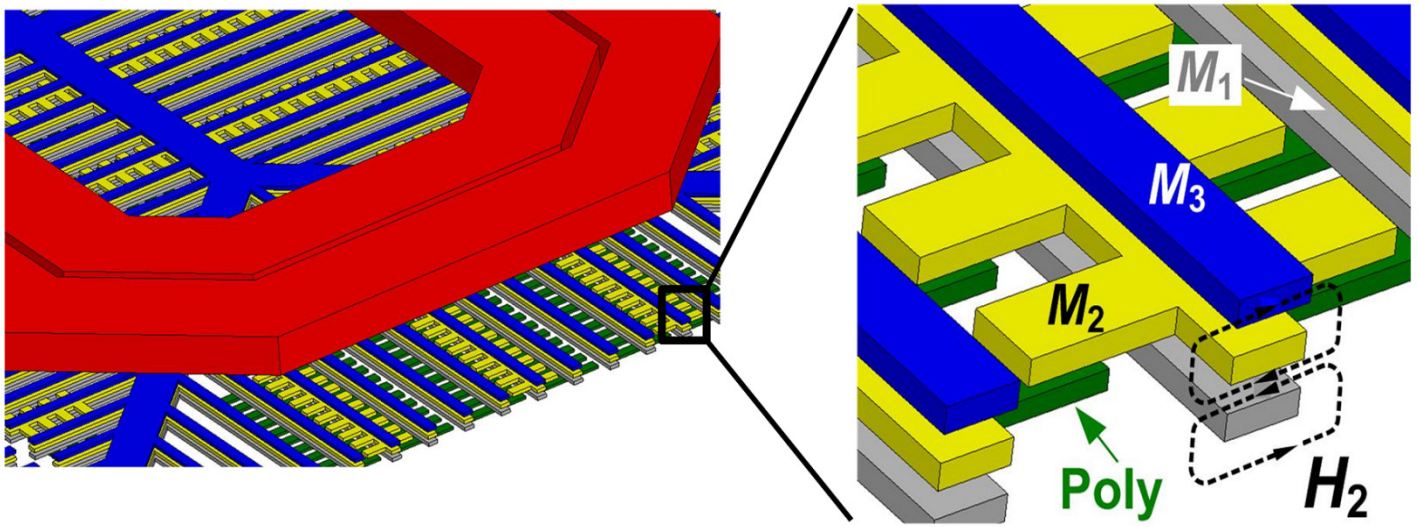


Loop Filter under Inductor

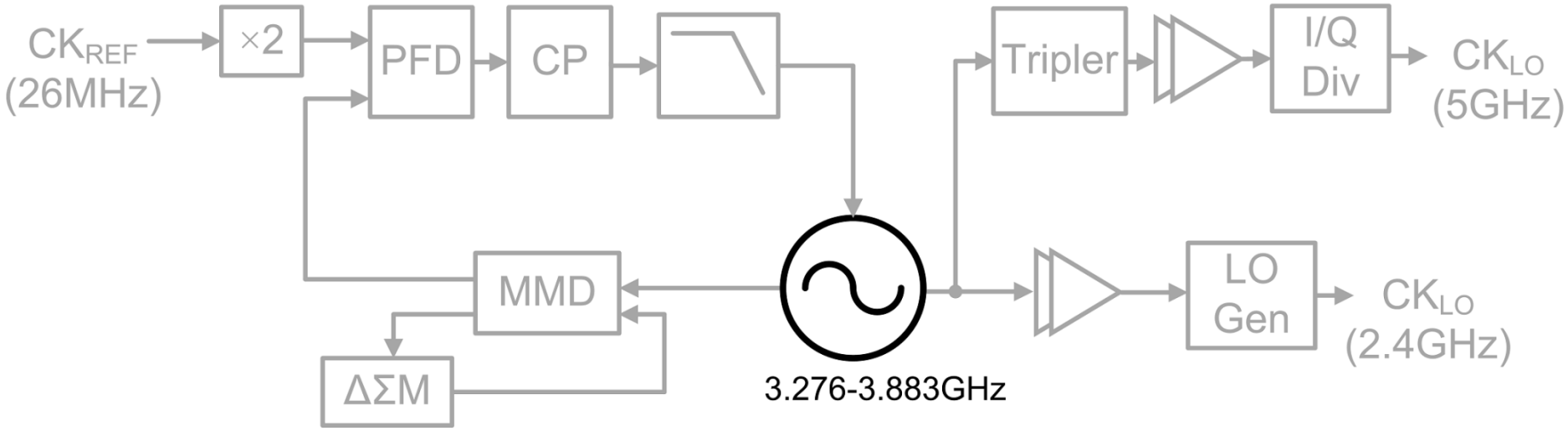


Any composite conductive loop would degrade inductor Q.

Capacitors are laid-out similar to a “fish-bone” structure.

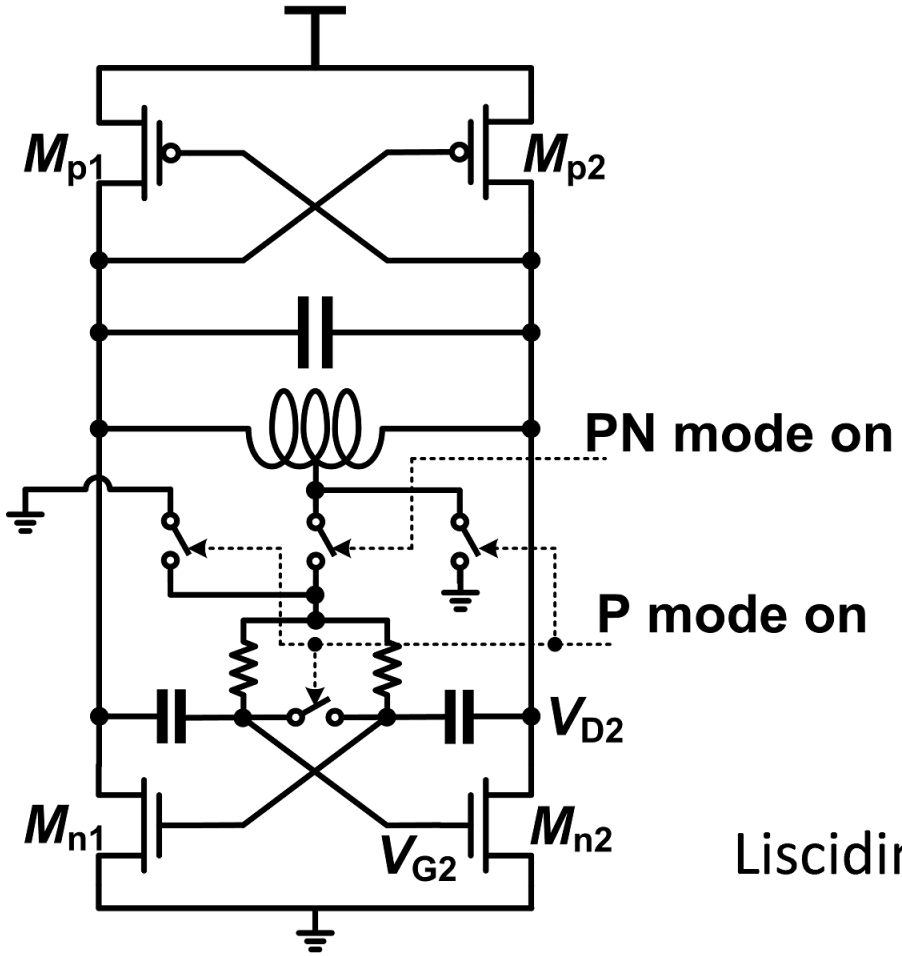


VCO



Reconfigurable VCO

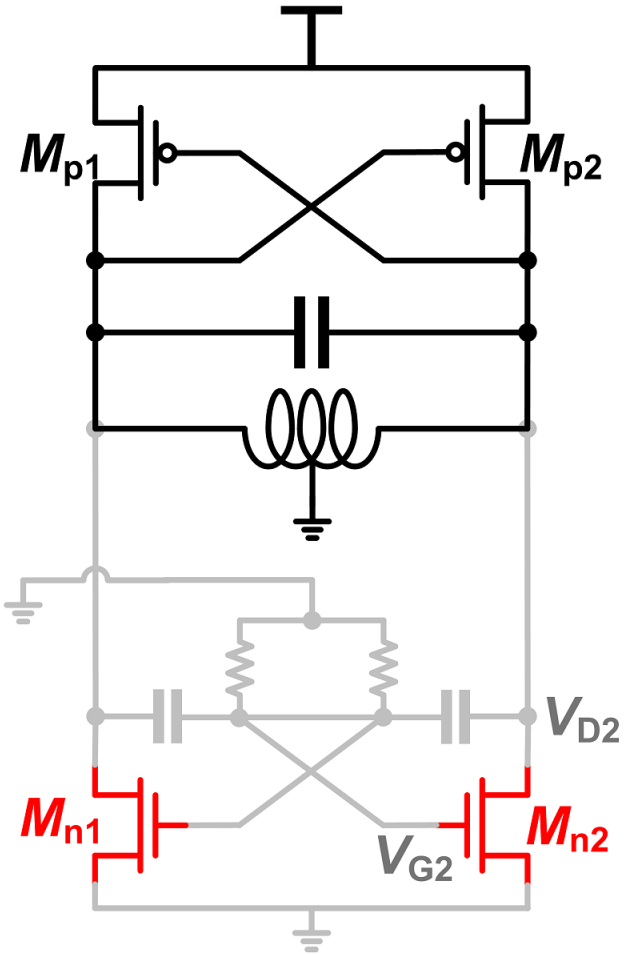
- PMOS topology (P mode) for high performance;
- CMOS topology (PN mode) for low power.

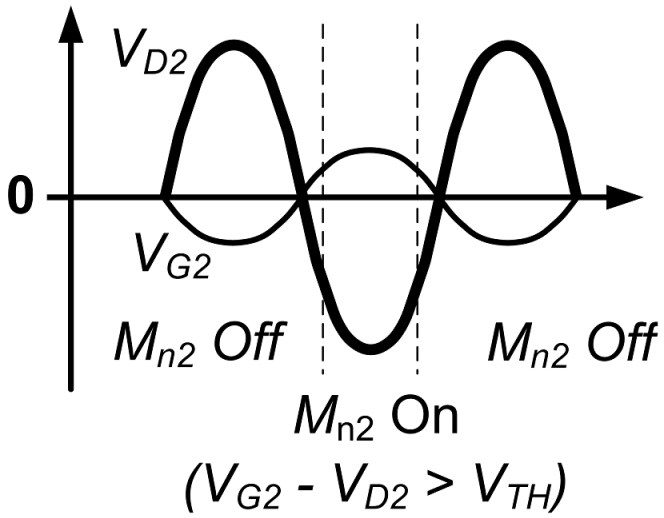


Liscidini, ISSCC 2012

High-Performance Mode

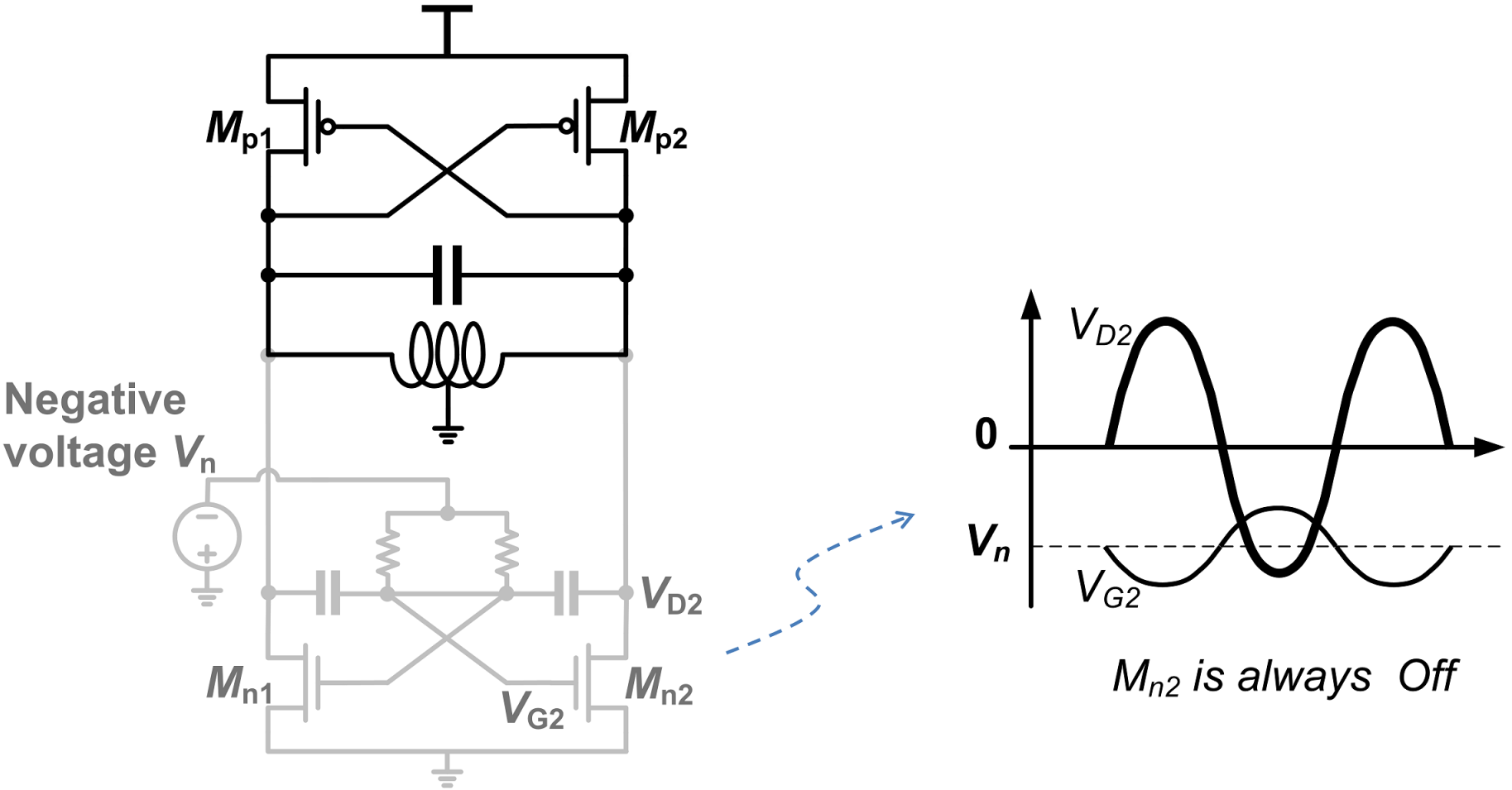
- When VCO swing is large enough, M_{n1} and M_{n2} are momentarily ON and degrade the tank Q.



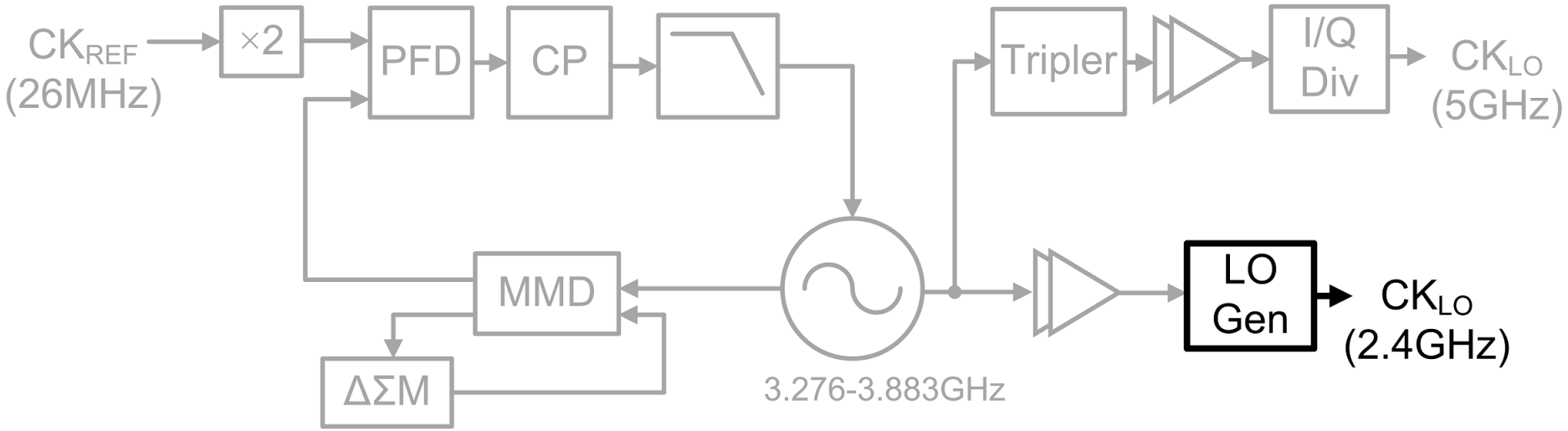


Biasing for High-Swing Case

- NMOS remain OFF in a complete VCO cycle. It helps increase tank's Q by 10% in our case.

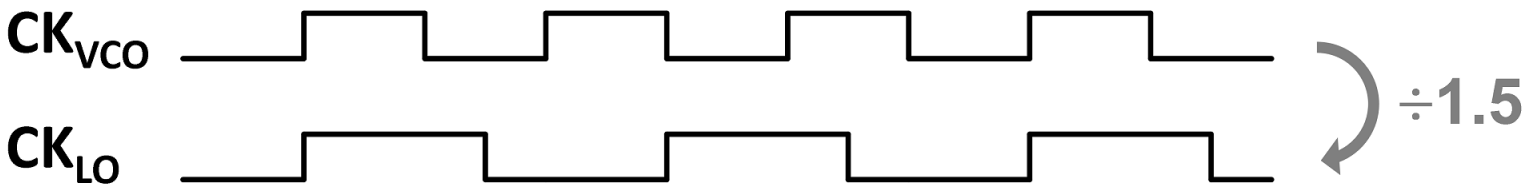


LO Generation



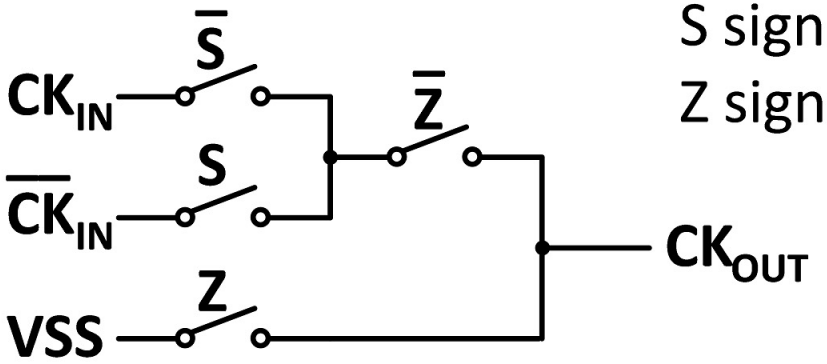
LO Generation

- Typical RF frequency synthesizers have
  $F_{VCO} = M \cdot F_{LO}$, where M is non-integer
  to avoid PA→VCO pulling.
- LO generation: Convert F_{VCO} to $F_{LO.}$

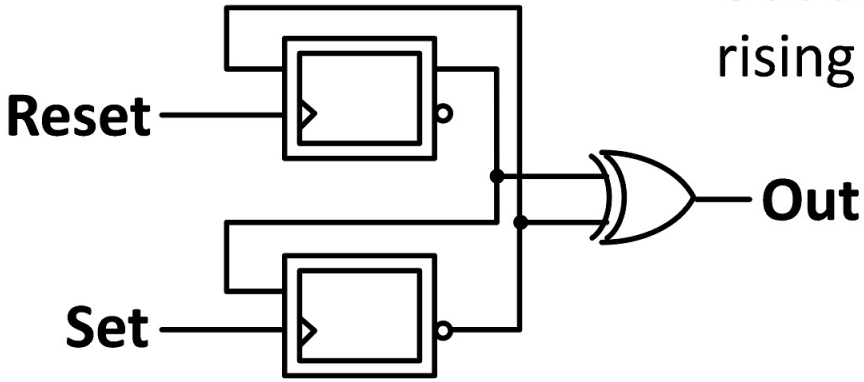


- Inductor-less LO generation
  - Avoid magnetic coupling with nearby LC-tanks.
  - Much smaller area.

Building Blocks of LO Generation

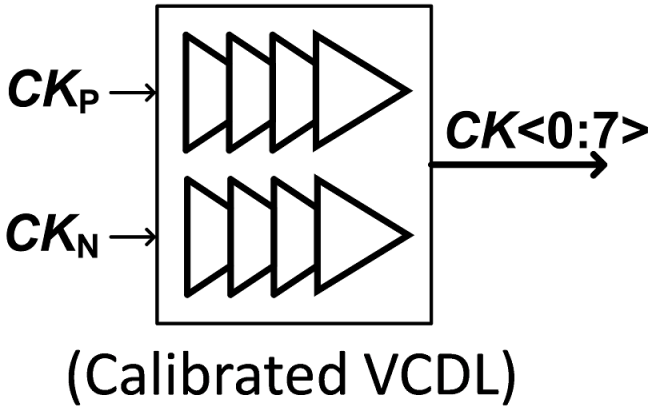


S signal selects the clock phase.
Z signal determines whether to output clock.

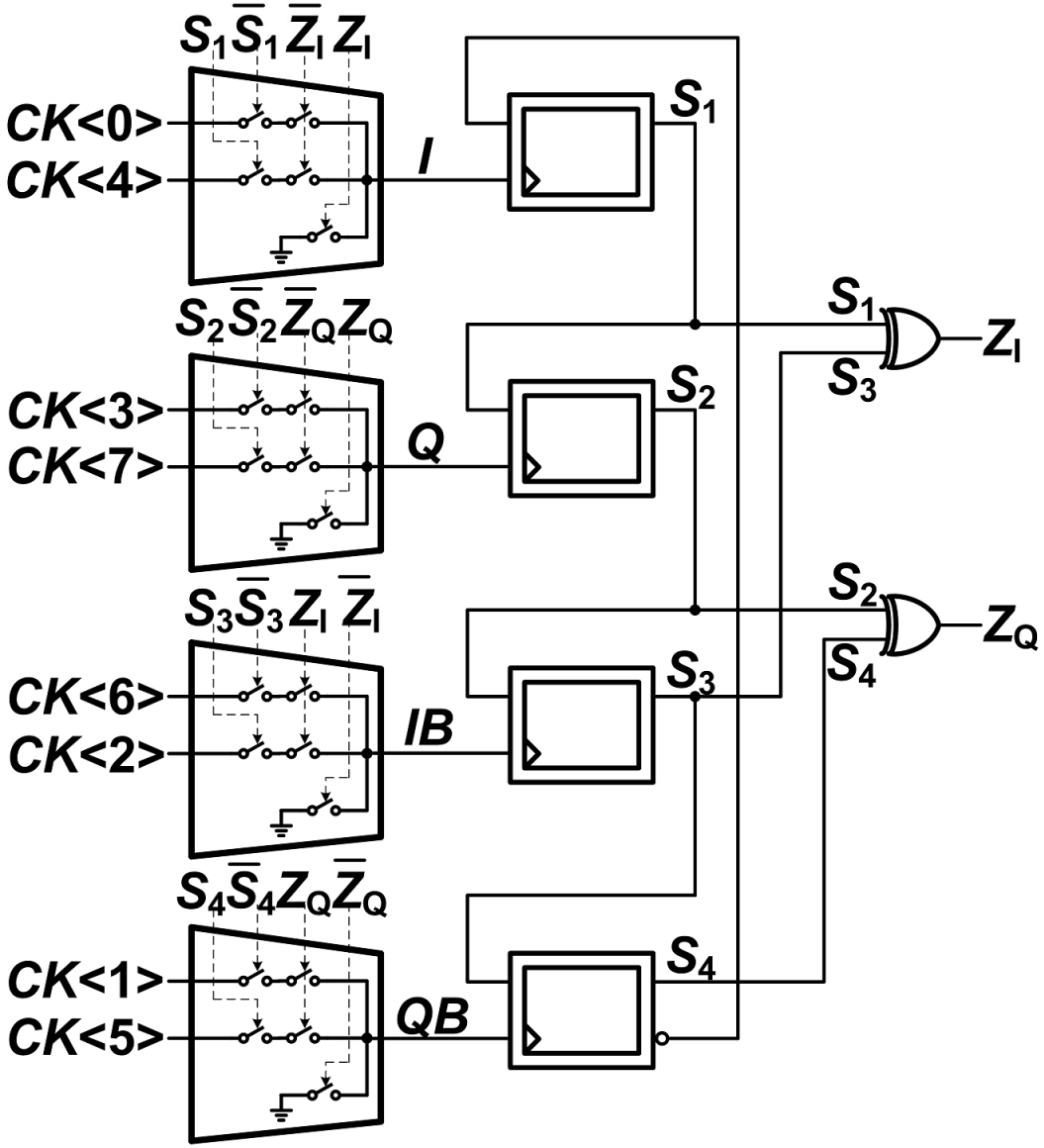


Out signal is “set” or “reset” at rising edges of input signals.

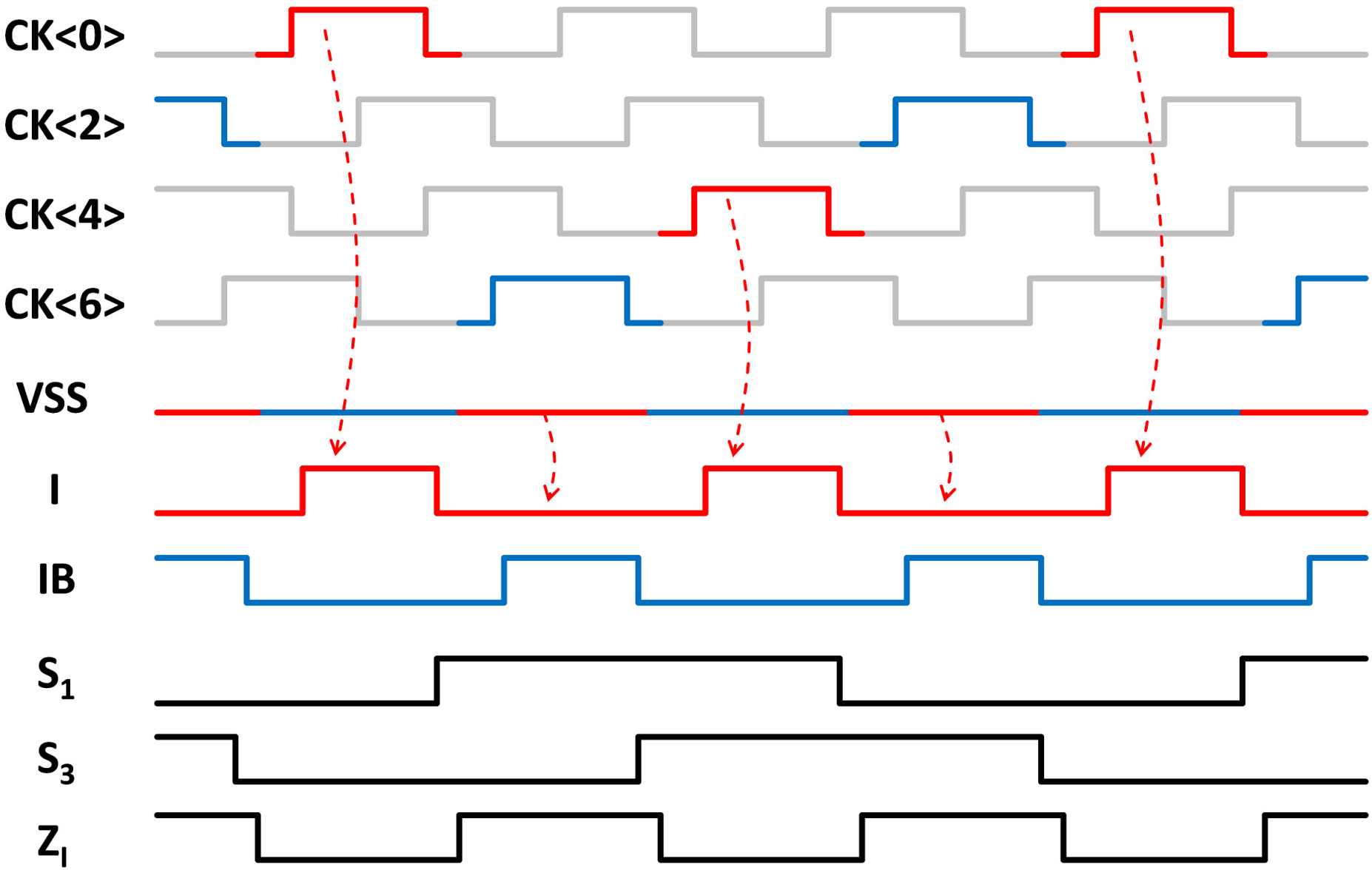
Inductor-Less LO Generation



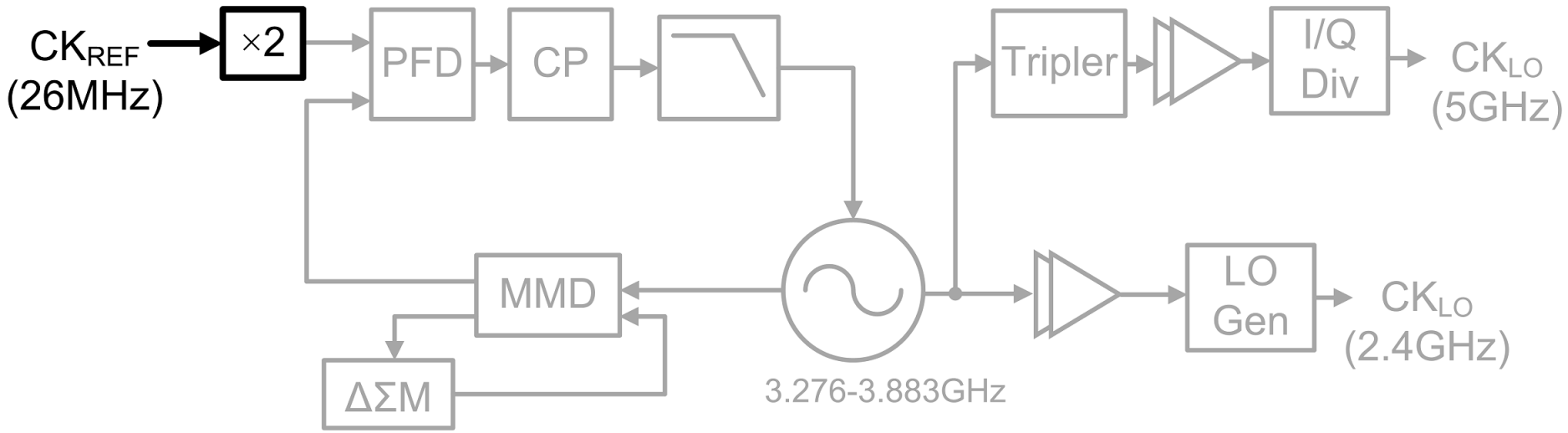
(Calibrated VCDL)



Clock Synthesis

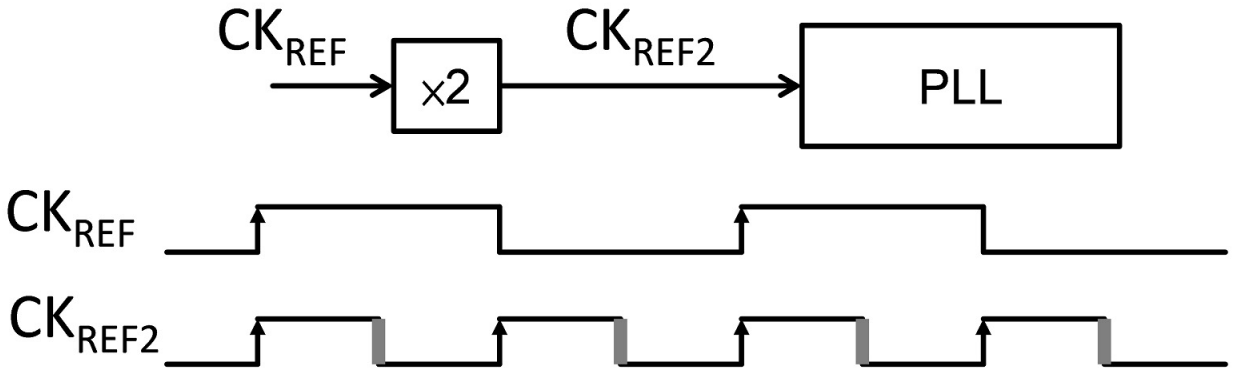


Reference Clock Doubler



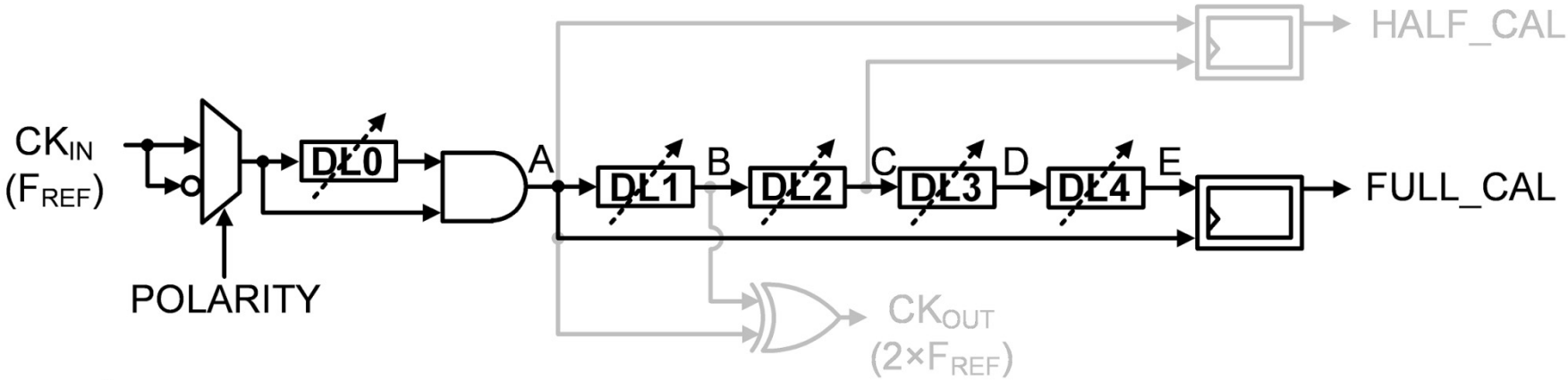
Reference Clock Doubler

- Utilize both rising/falling edges of CK_{REF}.

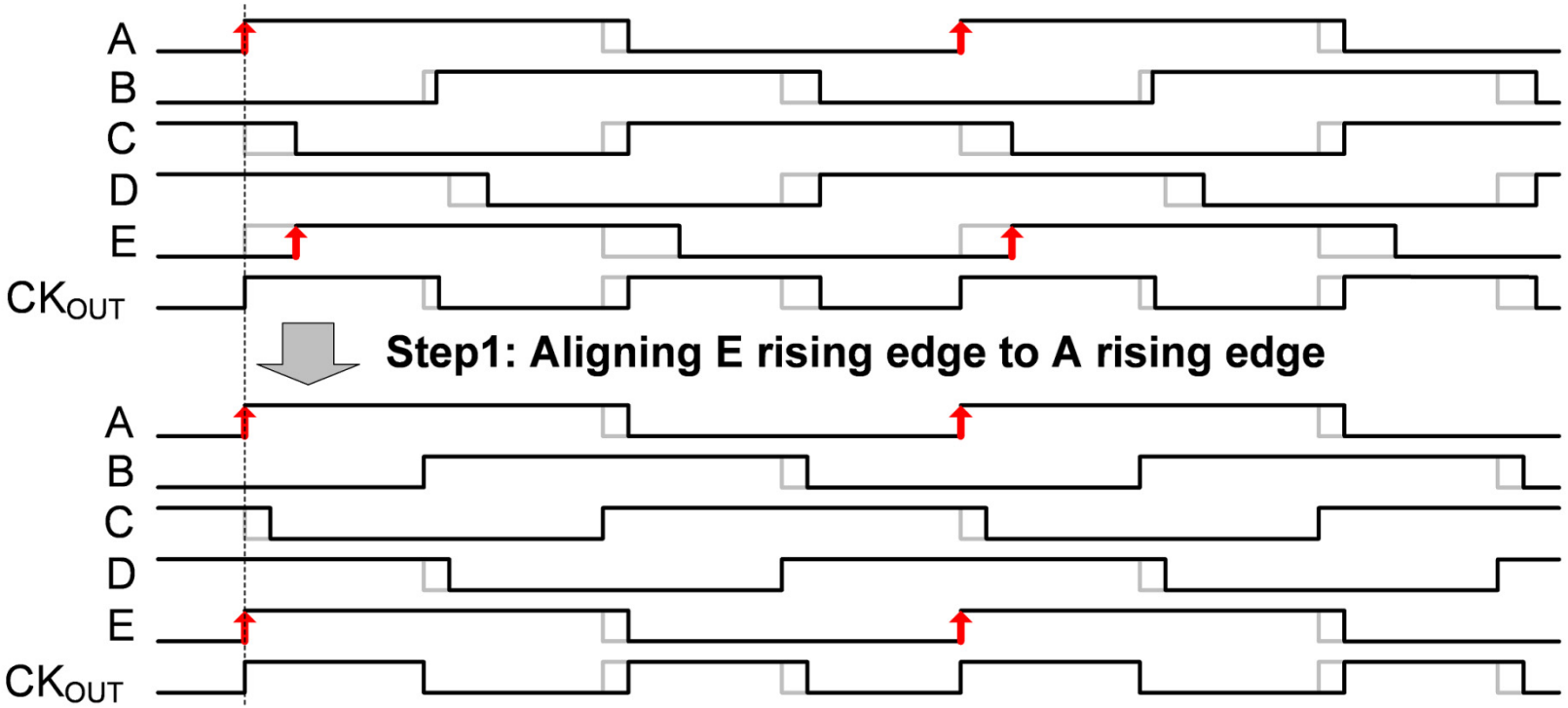


- Help improve PLL in-band noise.
- Need calibration to minimize reference spur.
- Proposed circuit
  - Fast calibration, by avoiding charge integration.
  - Relatively small area, by getting rid of integration cap. or LPF.

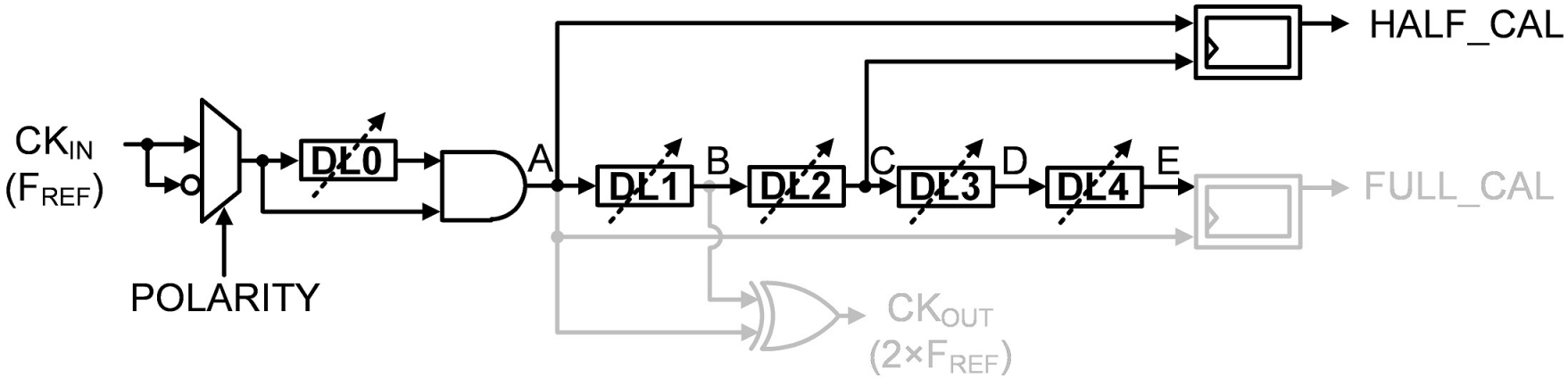
Calibration Step 1



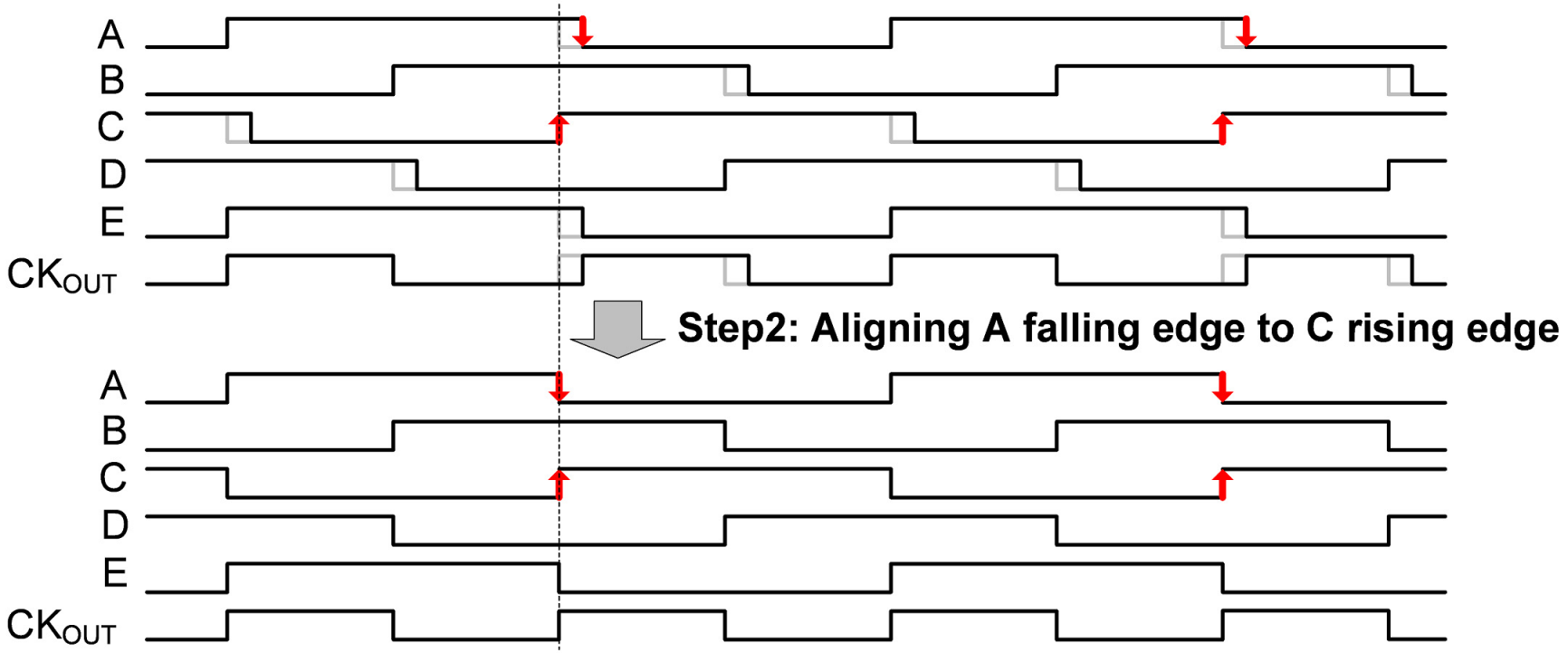
Adjust DL1~DL4



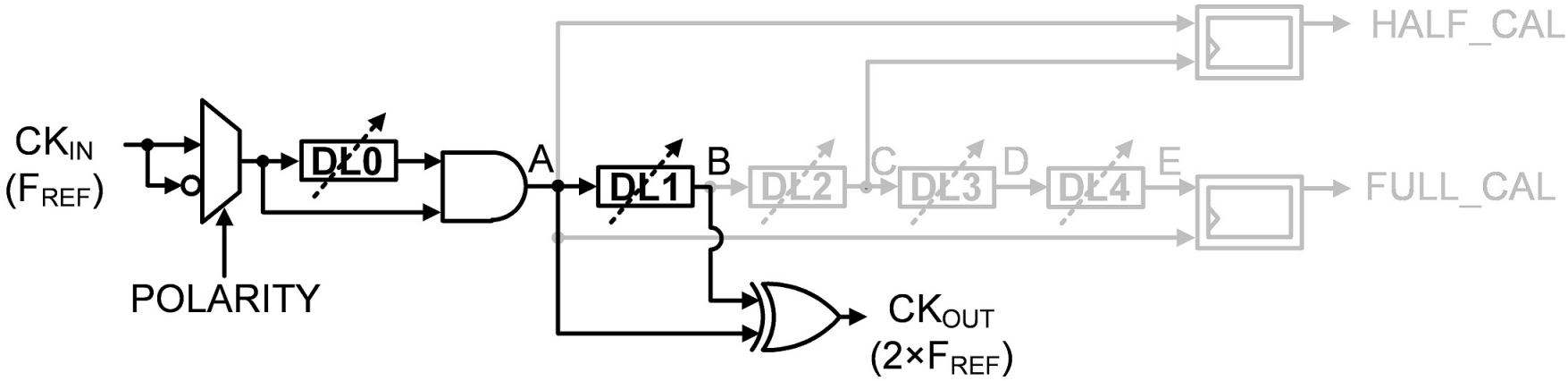
Calibration Step 2

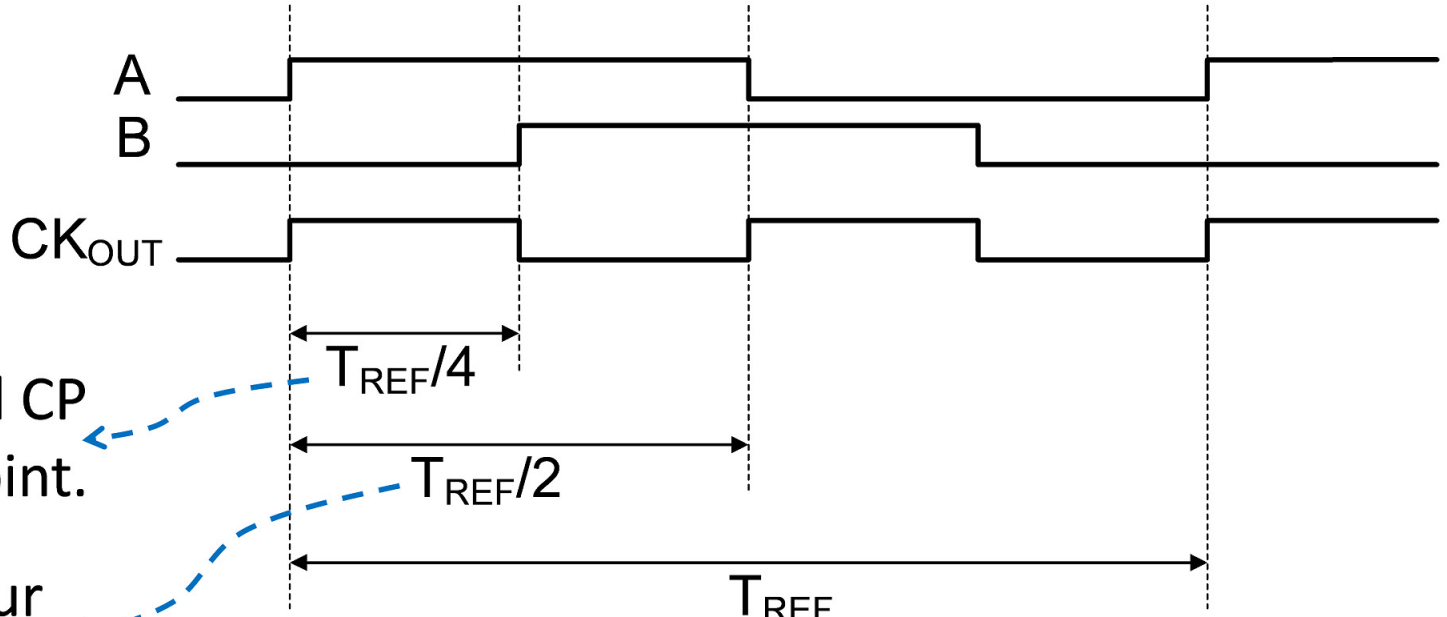


Set POLARITY and Adjust DL0



Calibration Completion



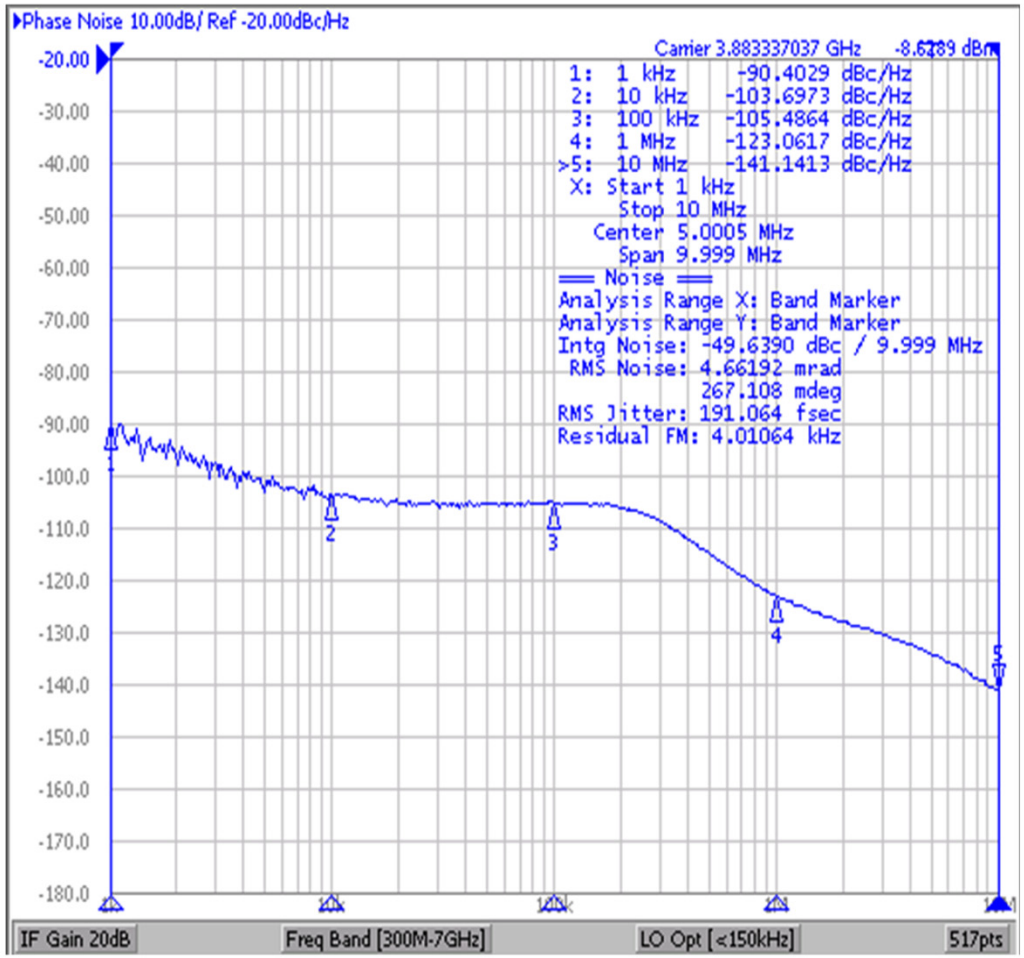


Well-defined CP operating point.

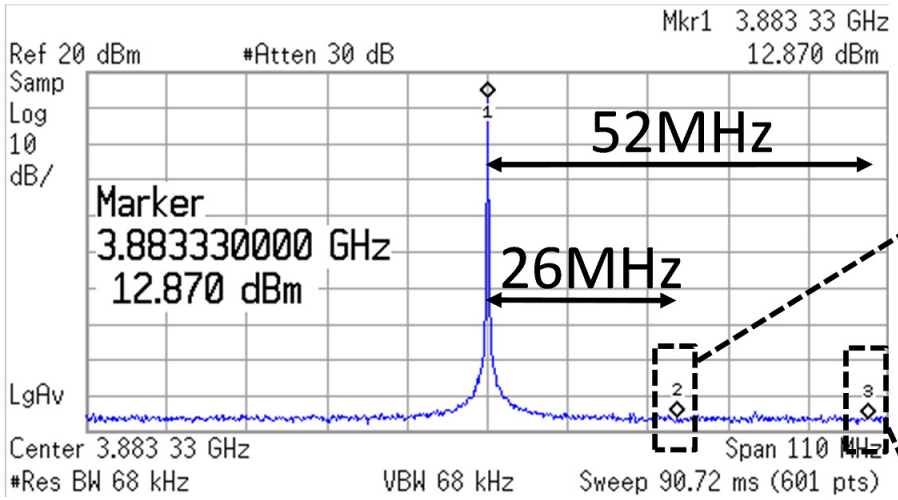
Minimize spur at F_{REF} offset.

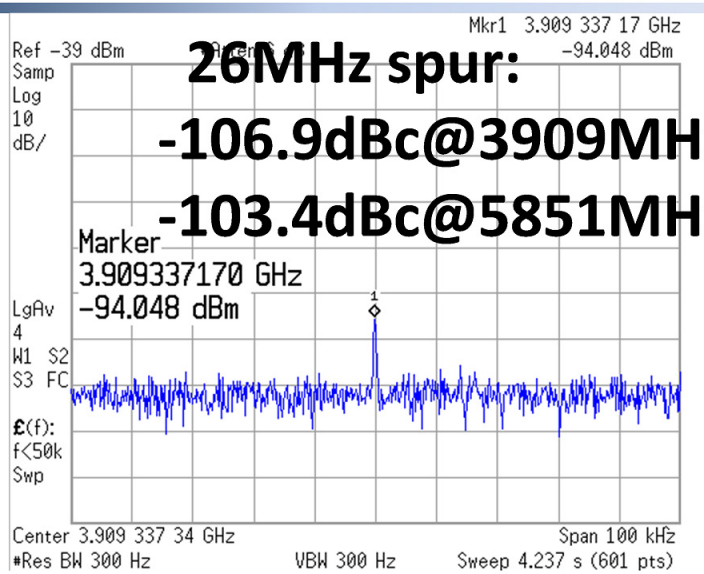
Measured Phase Noise Profile

- Jitter = 0.19ps$_{RMS}$ (1k-10MHz) for 802.11ac.

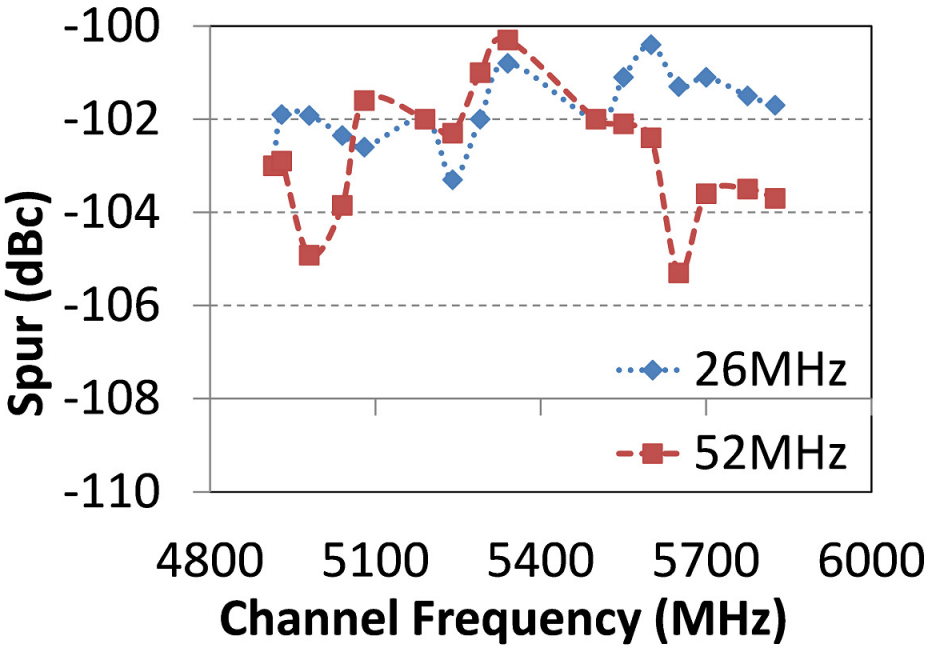


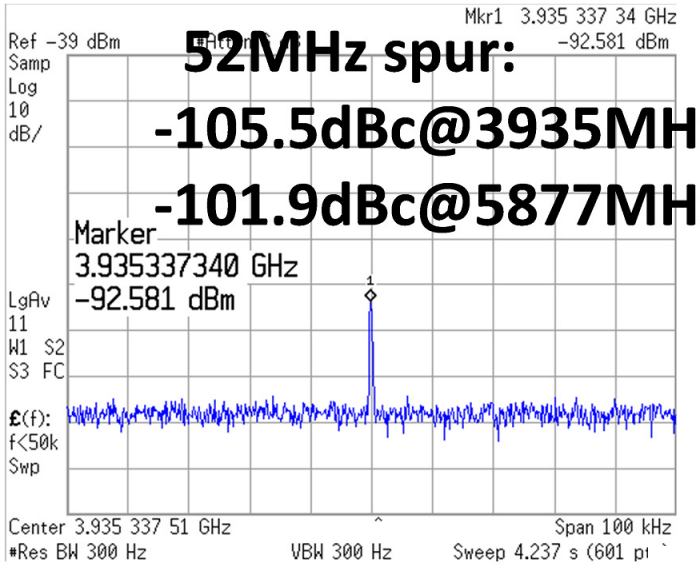
Reference Spur Measurement





26MHz spur:
-106.9dBc@3909MHz
-103.4dBc@5851MHz





52MHz spur:
-105.5dBc@3935MHz
-101.9dBc@5877MHz

Performance Summary Table

	Tasca. ISSCC'2011 pp.88-89	Yao. VLSI'2011 pp.110-111	Levantino. RFIC'2012 pp.177-180	Zhang. RFIC'2013 pp.119-122	This work
Process	65nm	55nm	65nm	130nm	**40nm LP w/o UTM**
Architecture	Digital	Digital	Analog	Analog	**Analog**
Normalized Reference Spur*	-61.2dBc	-86.5dBc	-60.2dBc	-63.7dBc	**-100dBc**
RMS Jitter	0.56ps	0.19ps	0.79ps	0.45ps	**0.19ps (ac/a) 0.30ps (b/g)**
Power	4.5mW	36mW	5mW	5.8mW	**17.5mW(ac/a) 7.2mW (b/g)**
FoM	-238.5dB	-238.9dB	-235.1dB	-239.3dB	**-242.0dB**
Area	0.22mm^2	0.68mm^2	0.22mm^2	0.3mm^2	**0.29mm^2**

* Reference spur levels are normalized to F_{LO}=5.83GHz and F_{REF}=26MHz.

Conclusions

- High-performance and area-efficient RF frequency synthesizer.
- Proposed techniques
  - **Charge pump:** compact, low spur;
  - **Loop filter:** area re-use;
  - **VCO:** improved biasing for high-swing;
  - **2.4GHz LO generation:** inductor-less;
    - VCDL calibration takes <1µs;
  - **Reference doubler:** compact, fast calibration;
    - Calibration takes <1.1µs;
  - Fast calibrations: can be triggered frequently.

A Frequency-Defined Vernier Digital-to-Time Converter for Impulse Radar Systems in 65nm CMOS

Yu-Hsien Kao, Chang-Ming Lai, Jen-Ming Wu,
Po-Chiun Huang, Ping-Hsuan Hsieh, Ta-Shun Chu

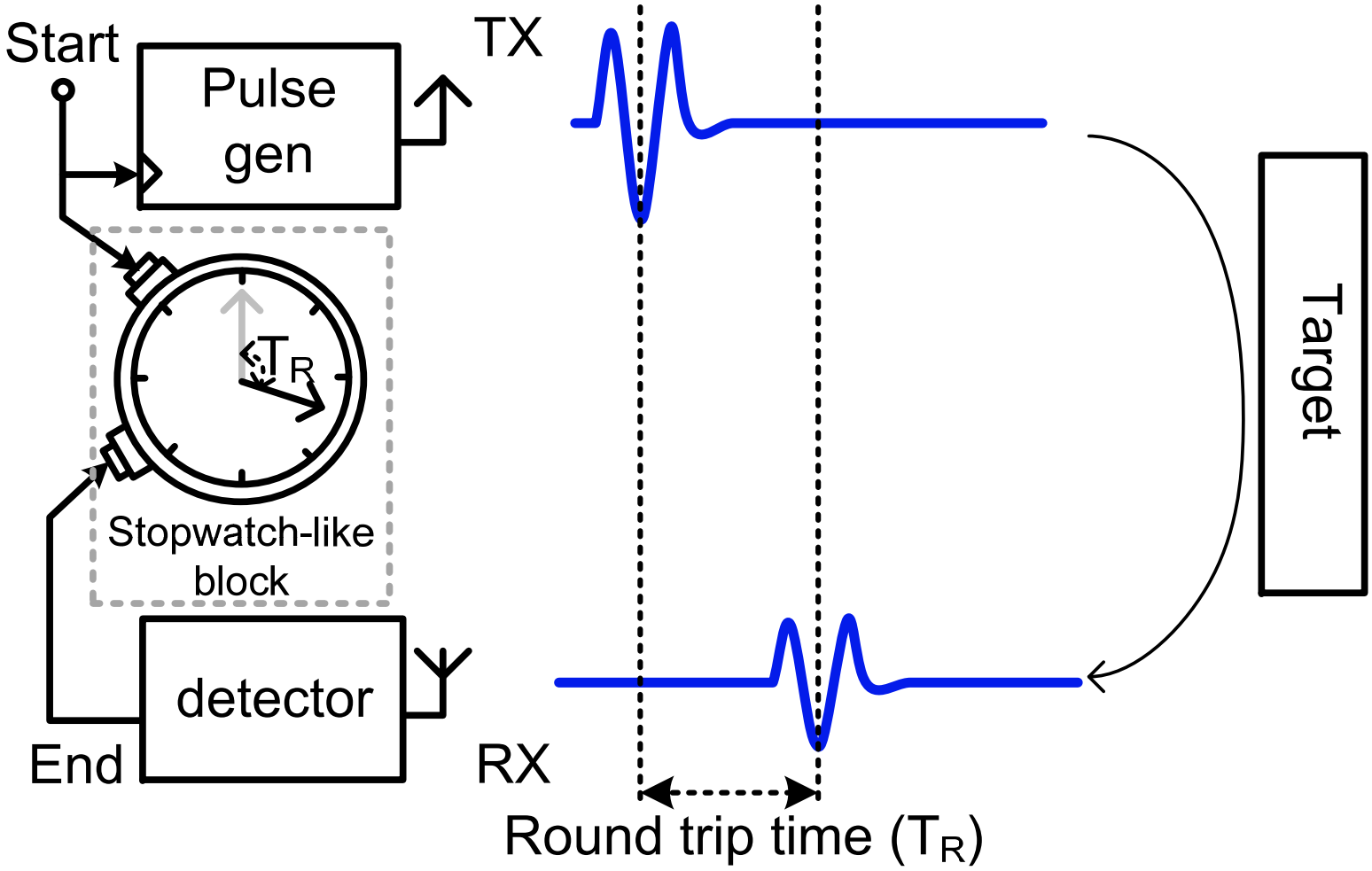
National Tsing-Hua University, Hsinchu, Taiwan

Outline

- Introduction
- Implemented direct-sampling radars
- Proposed frequency-defined Vernier DTC
- Circuit schematic of radar transceiver
- Measurement results
- Conclusions

Impulse Radar (Time-Of-Arrival)

- TOA is necessary to identify targets



Outline

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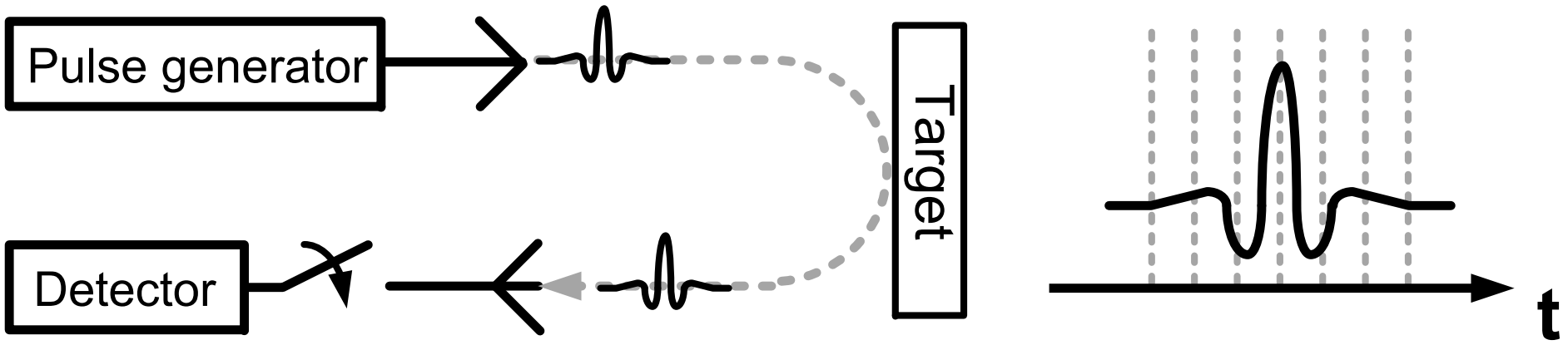
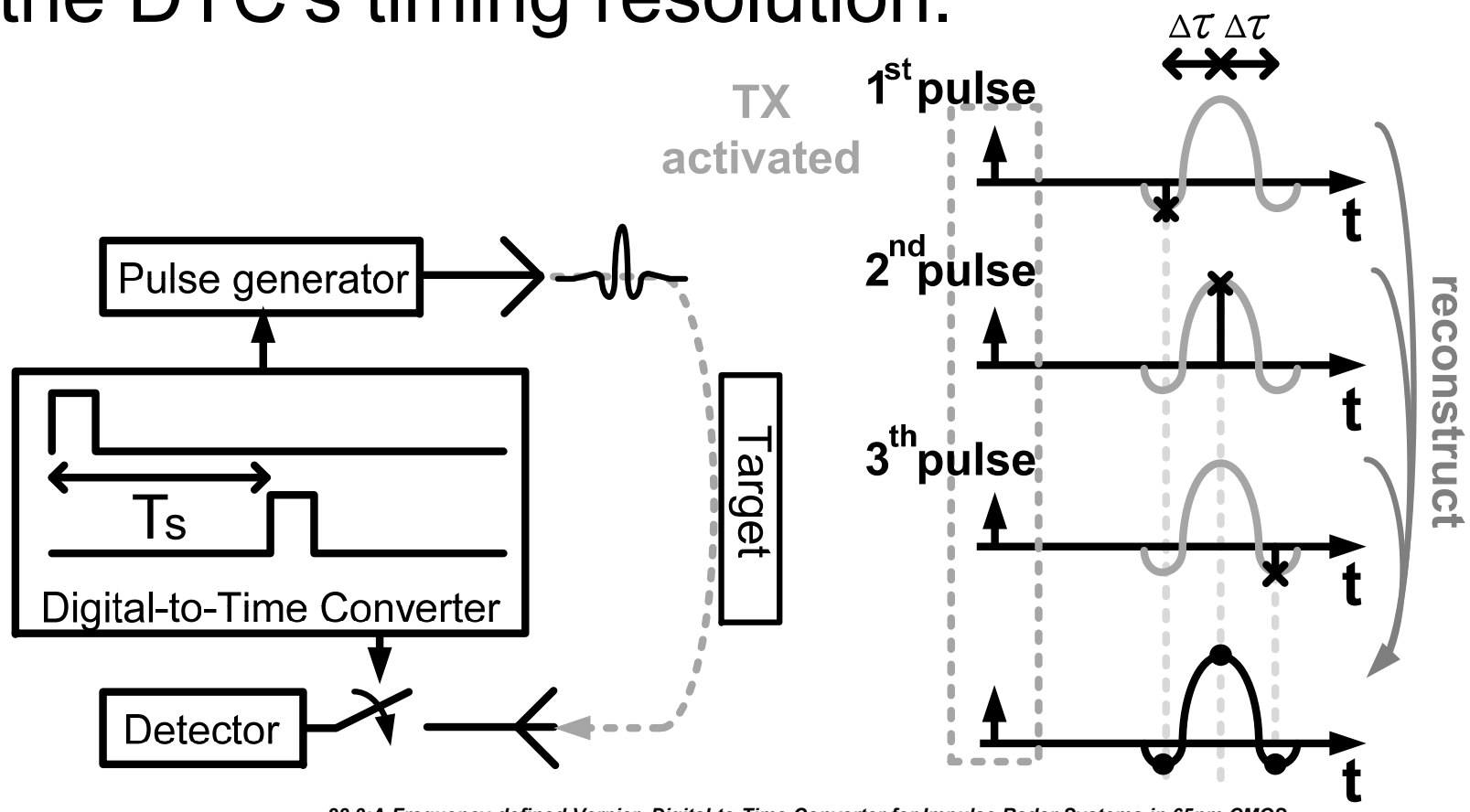
Direct-Sample Radar

- Reconstruct waveform
  - Sampling-based impulse radar
  - Higher sampling rates
- Quasi-stationary environment
  - Equivalent-time Sampling



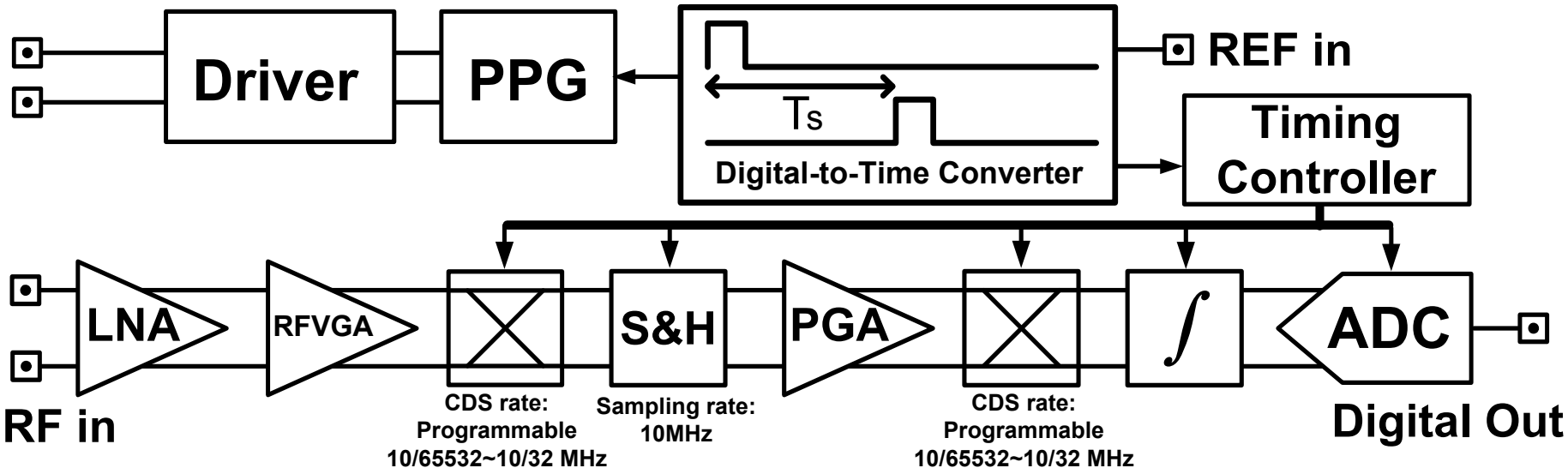
Equivalent-Time Sampling

- Sample signal at lower frequency.
- The radar range accuracy is decided by the DTC's timing resolution.



Block Diagram of Implemented Radar

- Features of the direct-sampling radar
  - Equivalent-time sampling technique
  - Reconstruct scattering waveform
  - SNR improvement
  - Correlated double sampling



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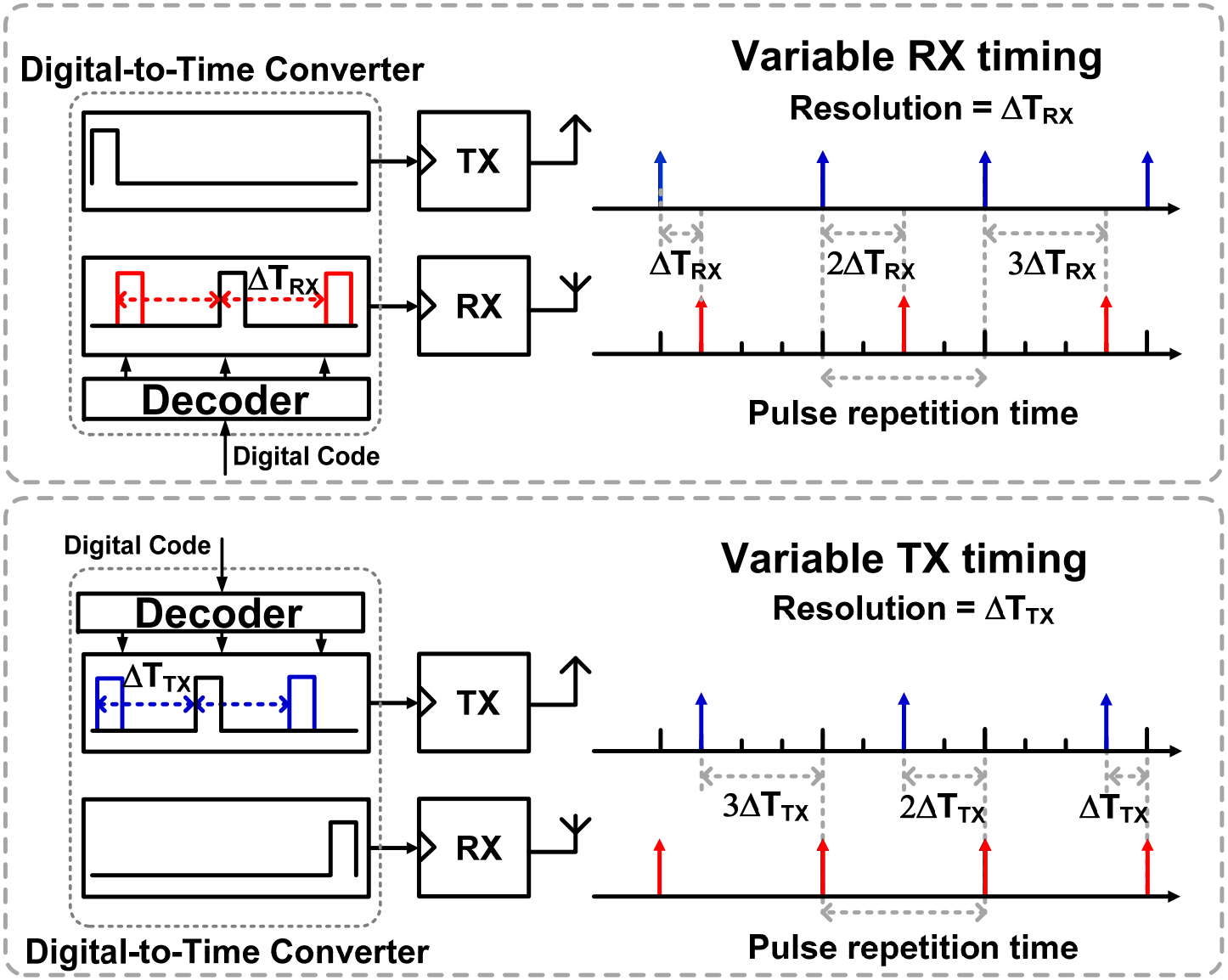
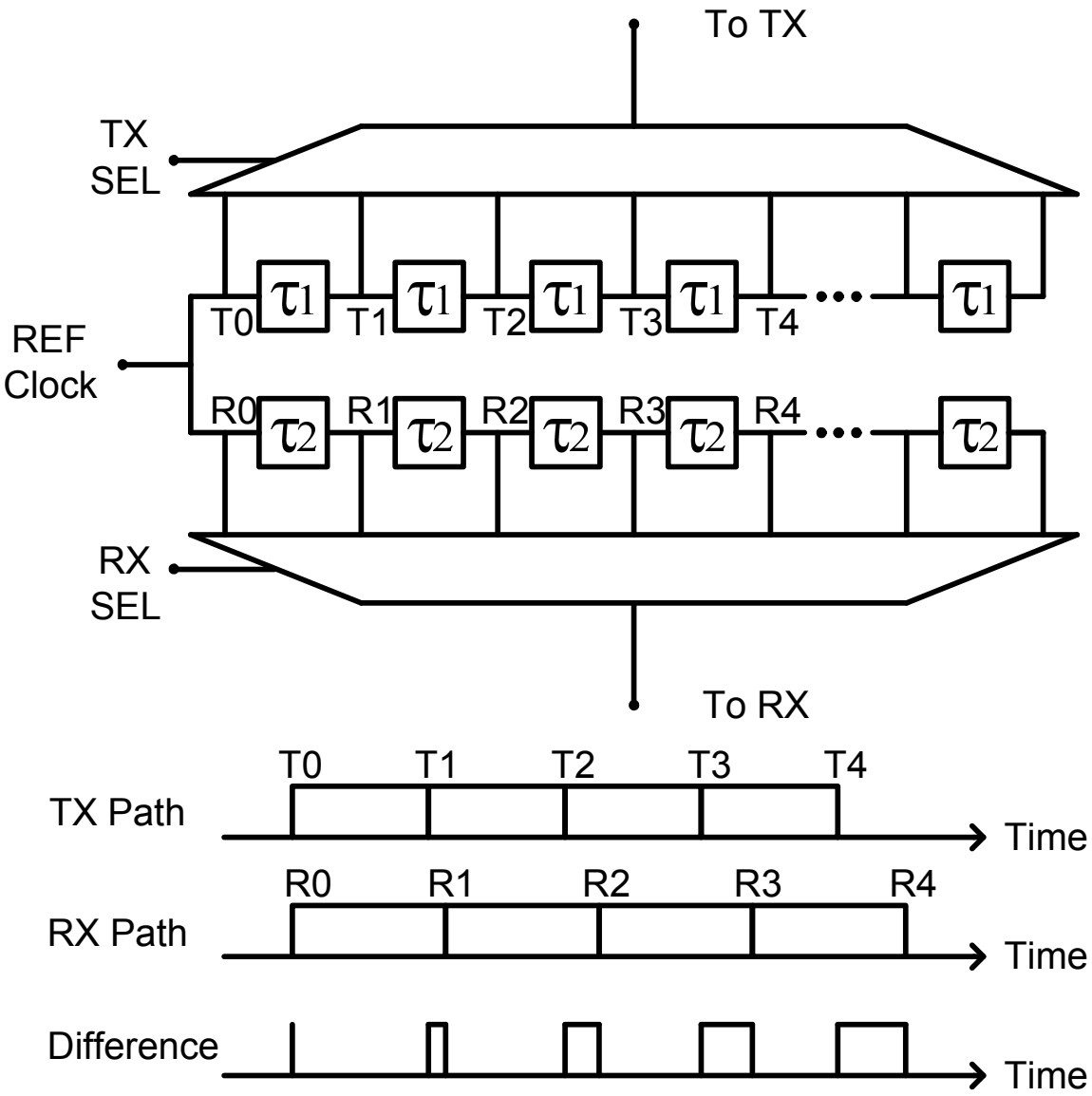
Digital-to-Time Converter

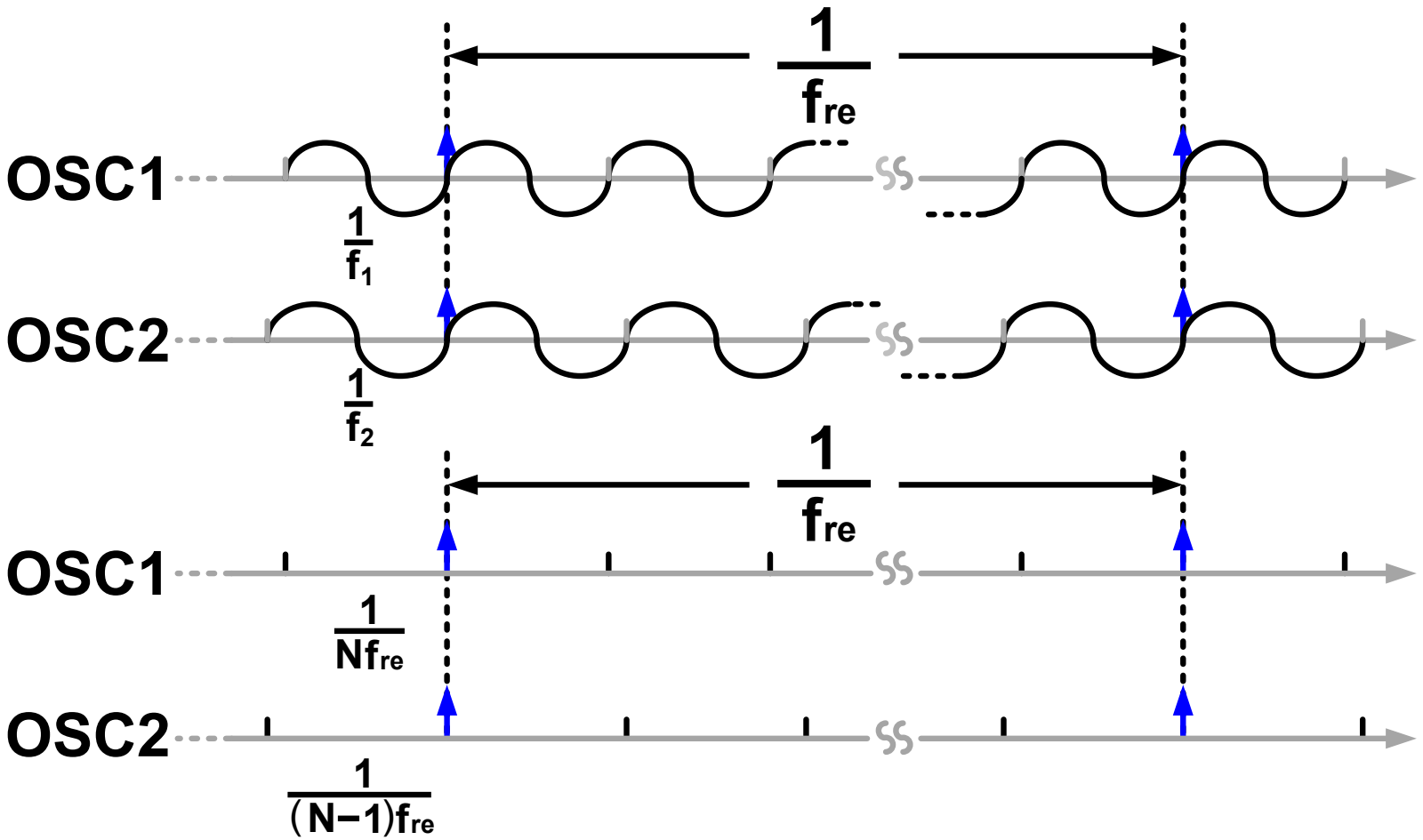


Digital-to-Time Converter



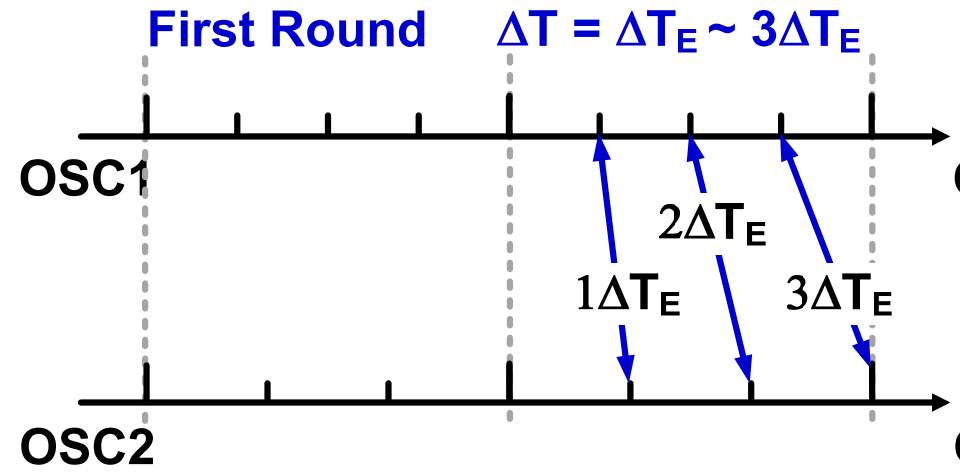
Frequency-Defined Vernier Delay Line

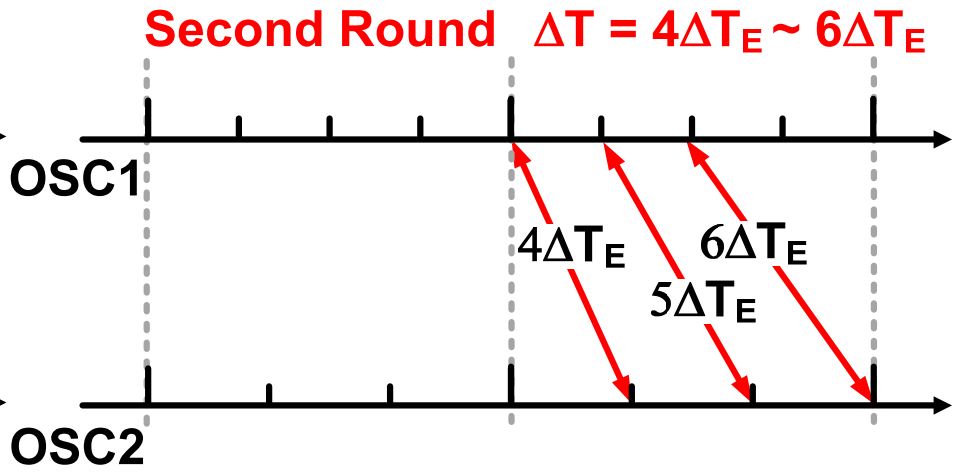
- $f_{re} = GCF(f_1, f_2)$
  - set $f_1 = Nf_{re}$, $f_2 = (N-1)f_{re}$

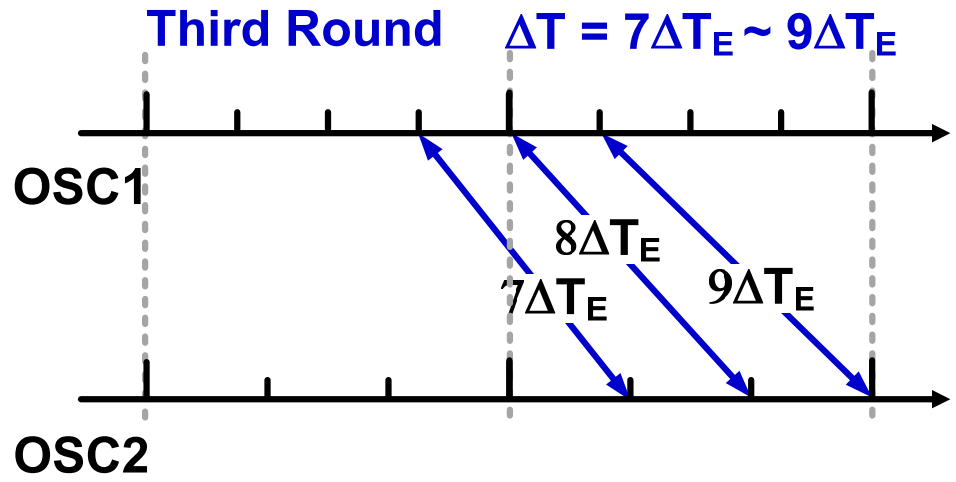


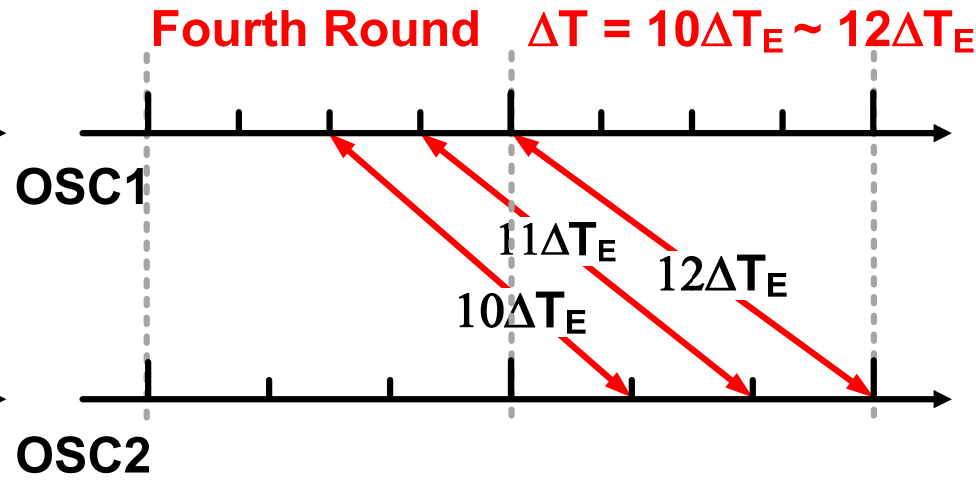
Frequency-Defined Vernier DTC (N=4)

- $\Delta T_E = \frac{1}{4\times 3 f_{re}} = \frac{1}{12 f_{re}}$



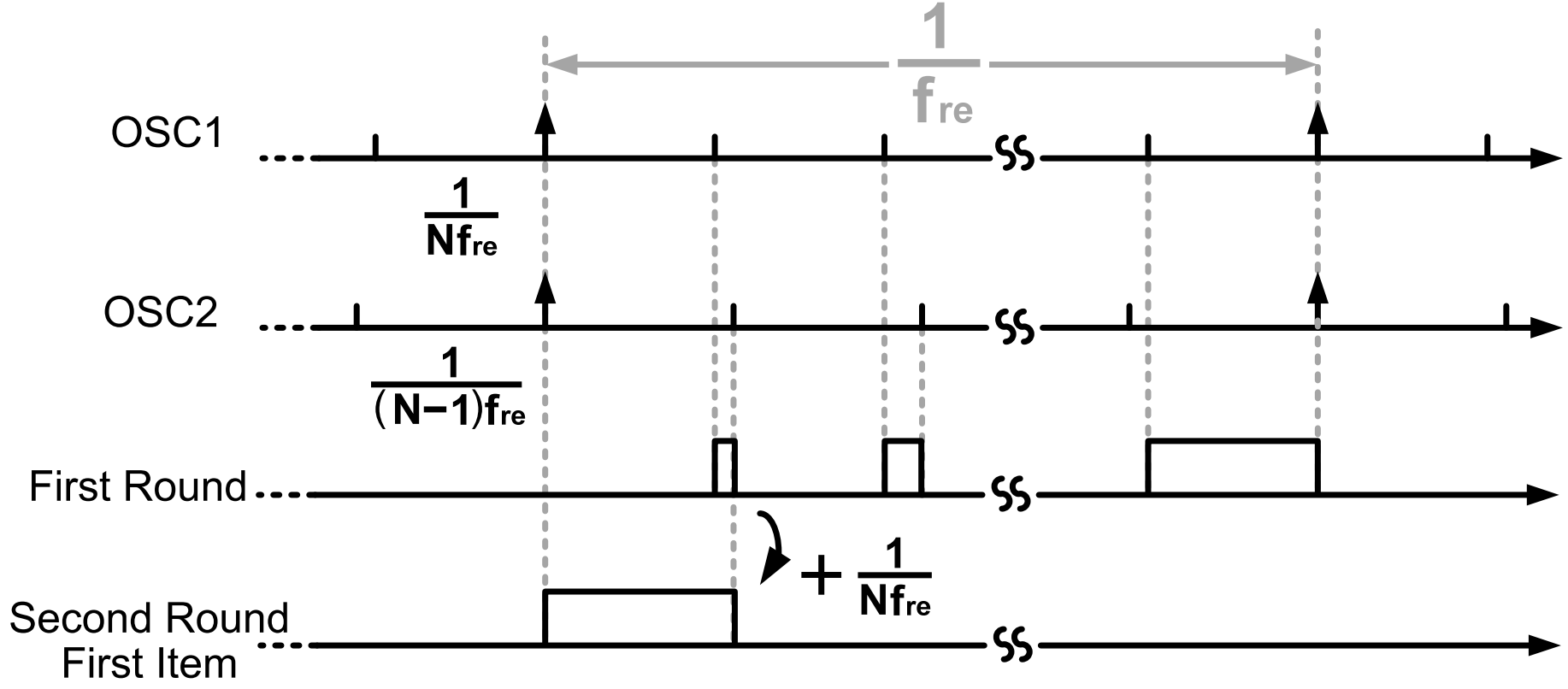






Frequency-Defined Vernier DTC

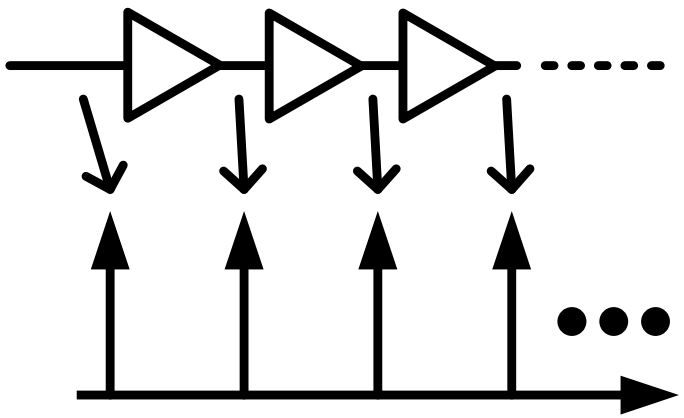
- Resolution : $\Delta = \frac{1}{N(N-1)f_{re}}$
- First round : $1\Delta \sim (N-1)\Delta$
- X-round : $1\Delta + (X-1)(N-1)\Delta \sim X(N-1)\Delta$



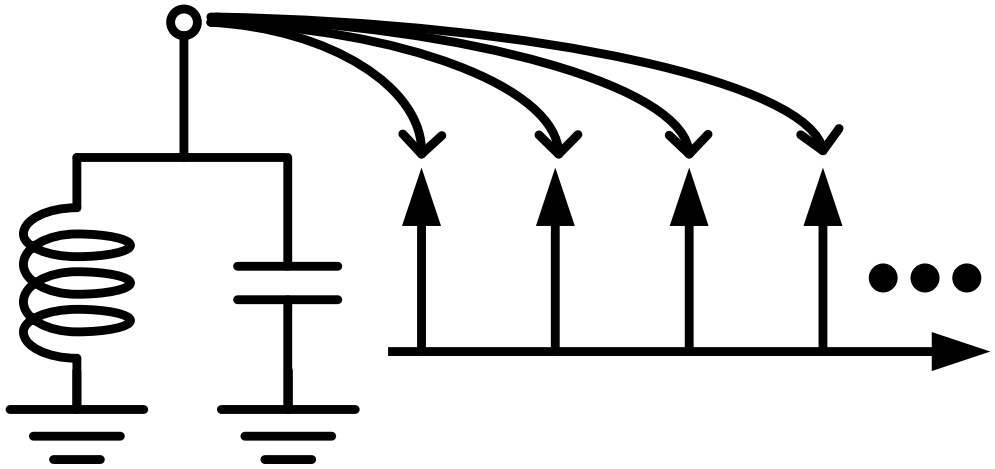
Frequency-Defined Vernier DTC

- Provide better resolution performance.
- Not Require a large number of delay cells.
- Inherently immune to device mismatch.

Conventional



Frequency-defined

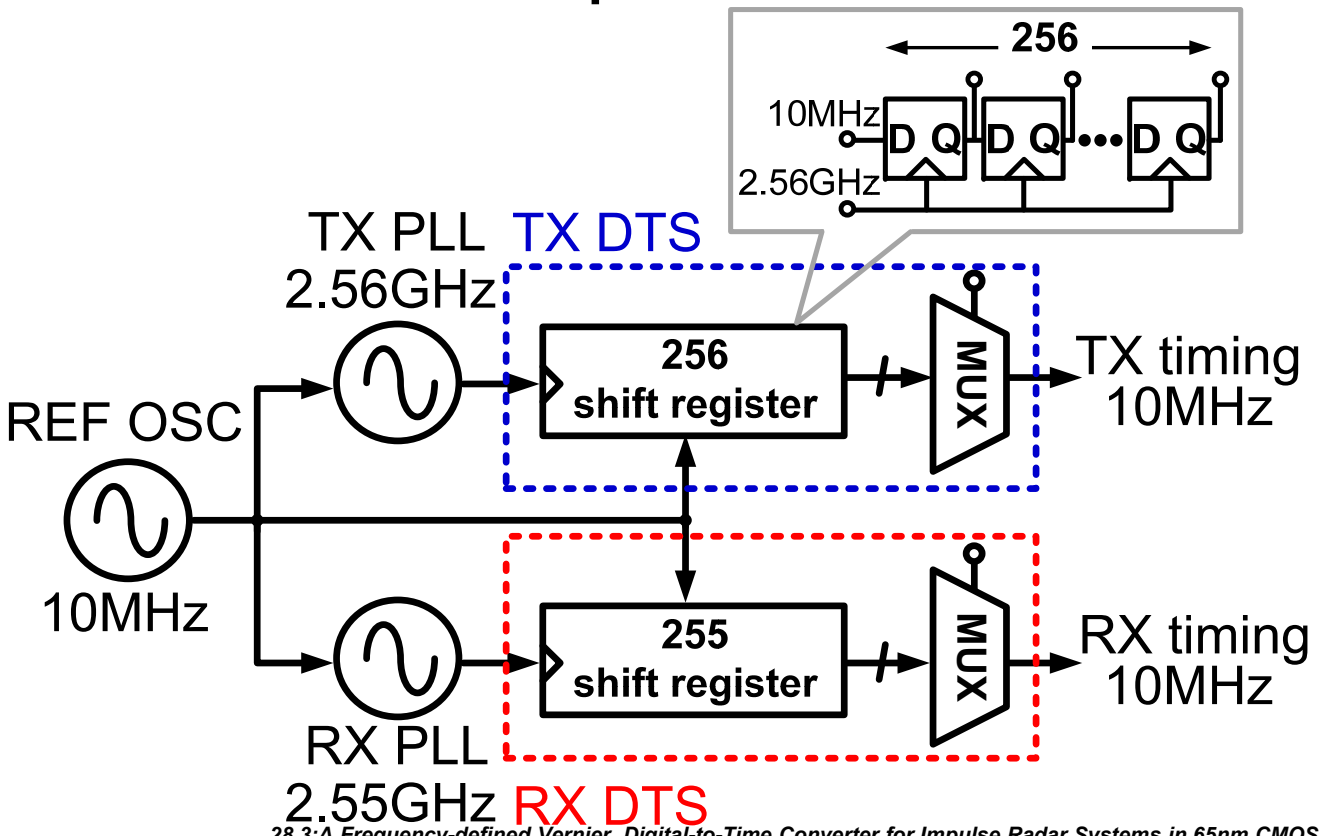


Design Goal

- Radar scanning range = 15 m
  - f_{re} = 10 MHz
  - Pulse repetition rate : 10MHz
- Radar range accuracy = 0.225 mm
  - Timing resolution : 1.53 ps
  - Equivalent sampling rate : ~666 GS/s
  - N = 256 → set f_{TX} = 2.56 GHz , f_{RX} = 2.55 GHz

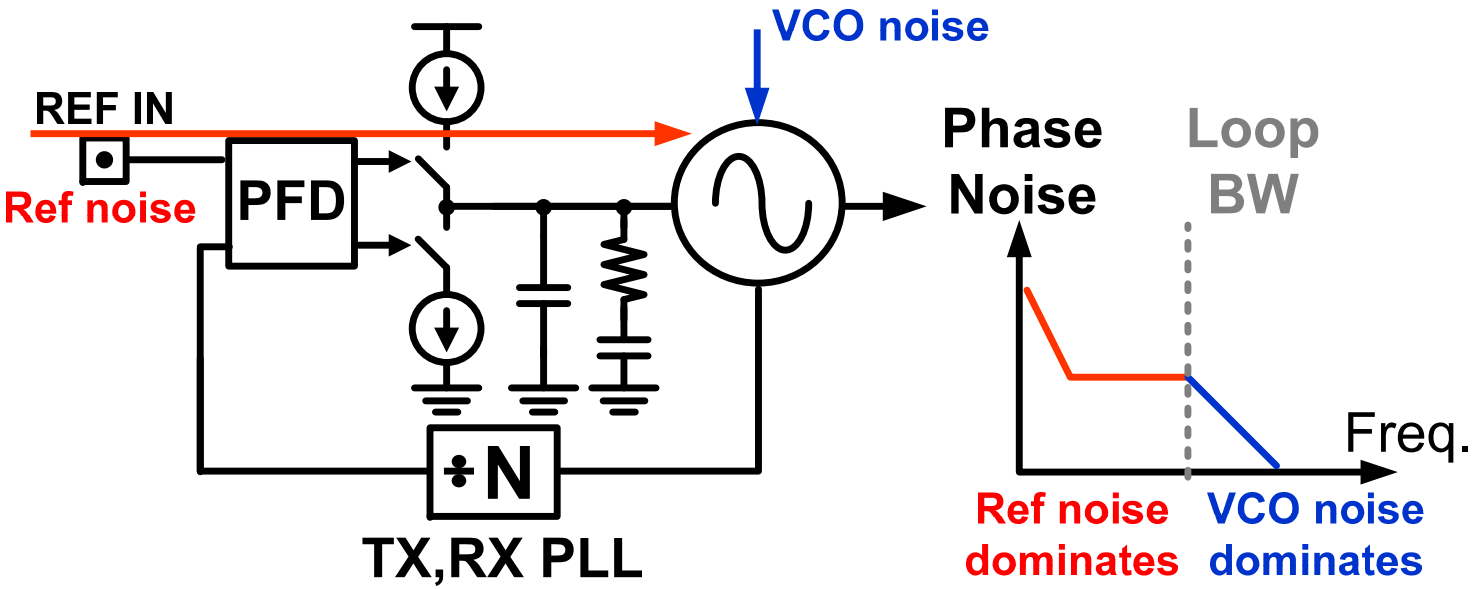
Simplified Block Diagram

- Precise resolution
- Insensitive PVT variation
- Instantaneous response



Noise Consideration : Synchronization

- Higher TX,RX PLL's loop bandwidth
- Higher reference frequency

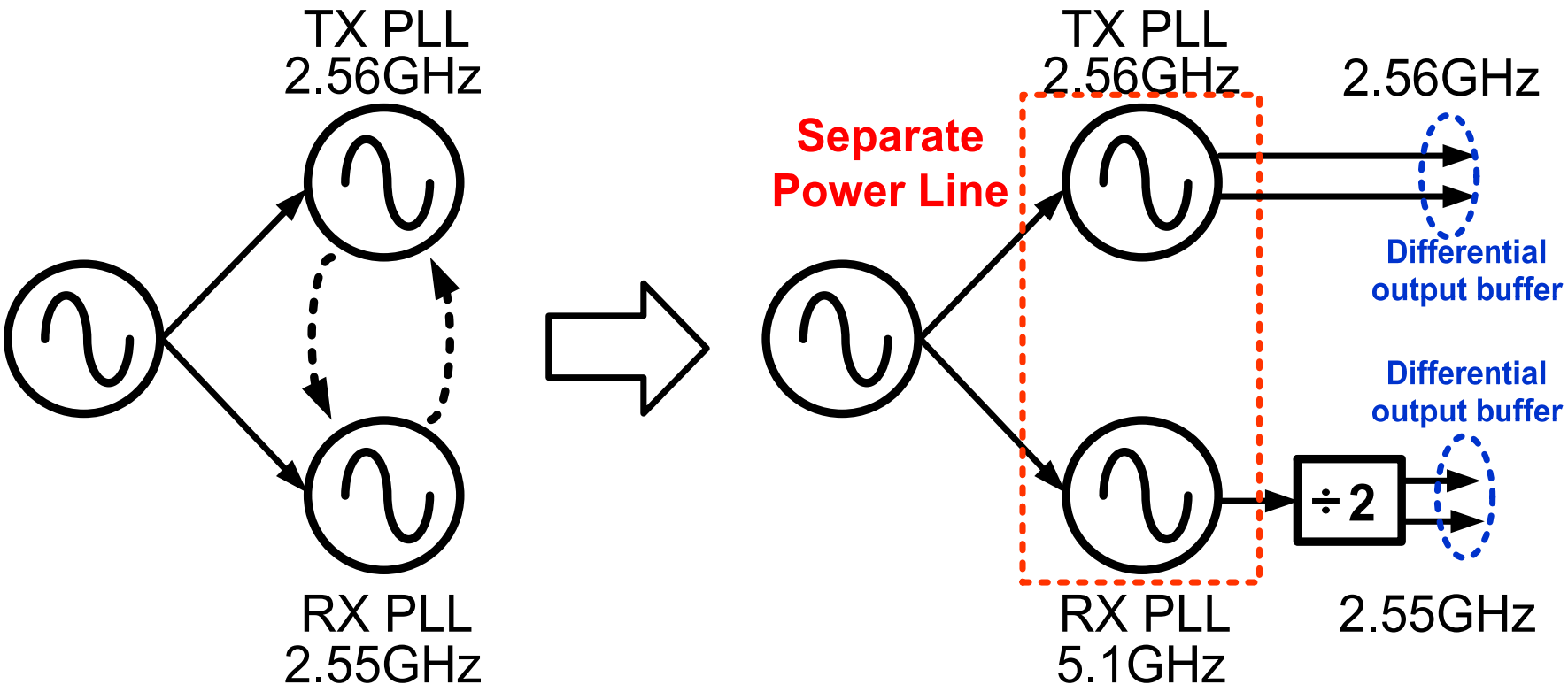


$$\Delta T = \Delta T_{sel} + T_{RX\&TX,vco,jitter}$$

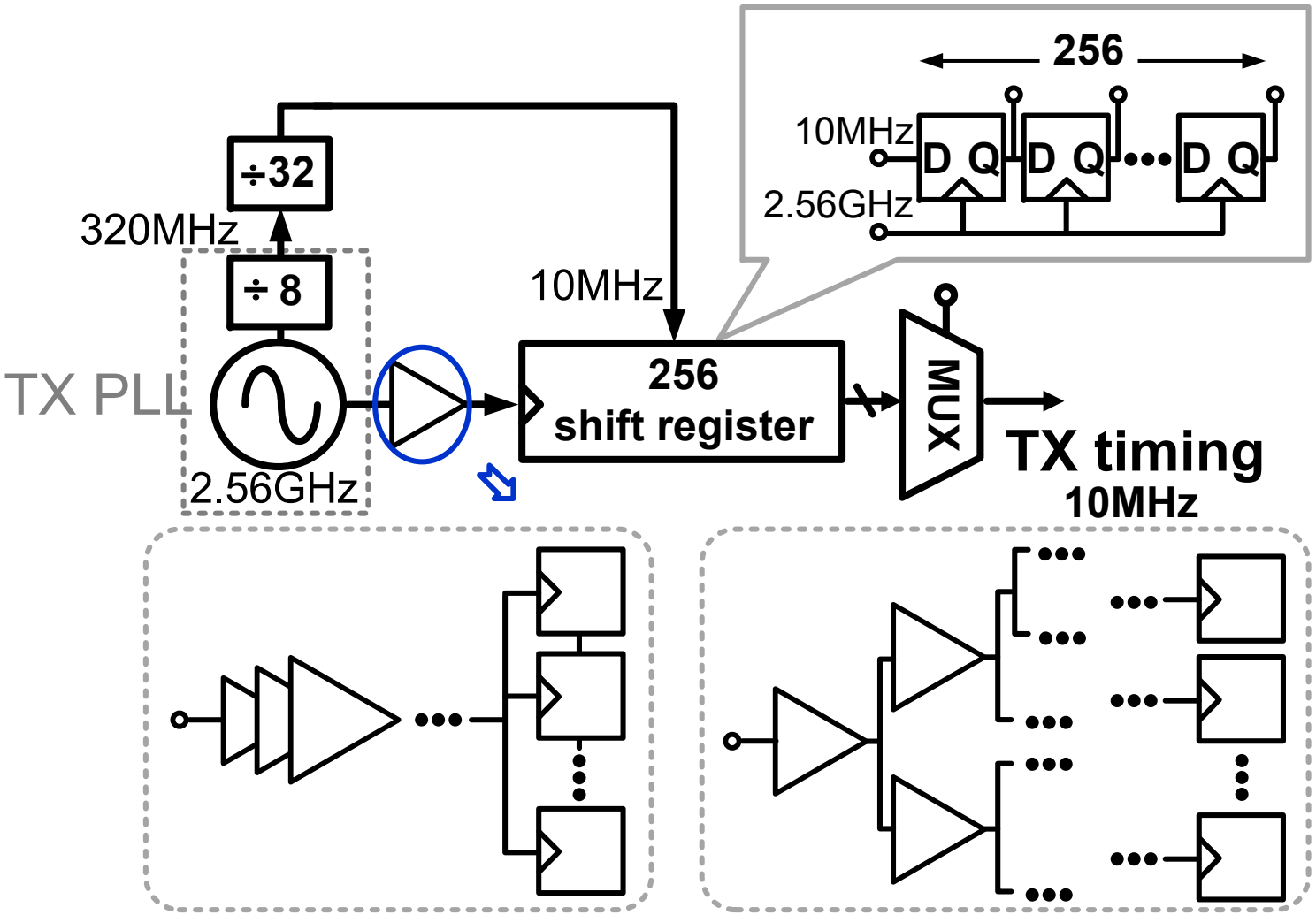
$$\Delta T = \left(T_{Rx} = T_{Rx,sel} + T_{ref,jitter} + T_{Rx,vco,jitter} \right) - \left(T_{Tx} = T_{Tx,sel} + T_{ref,jitter} + T_{Tx,vco,jitter} \right)$$

Frequency Plan between RX and TX PLL

- Double the frequency of RX PLL
- Differential buffer
- Separate power line



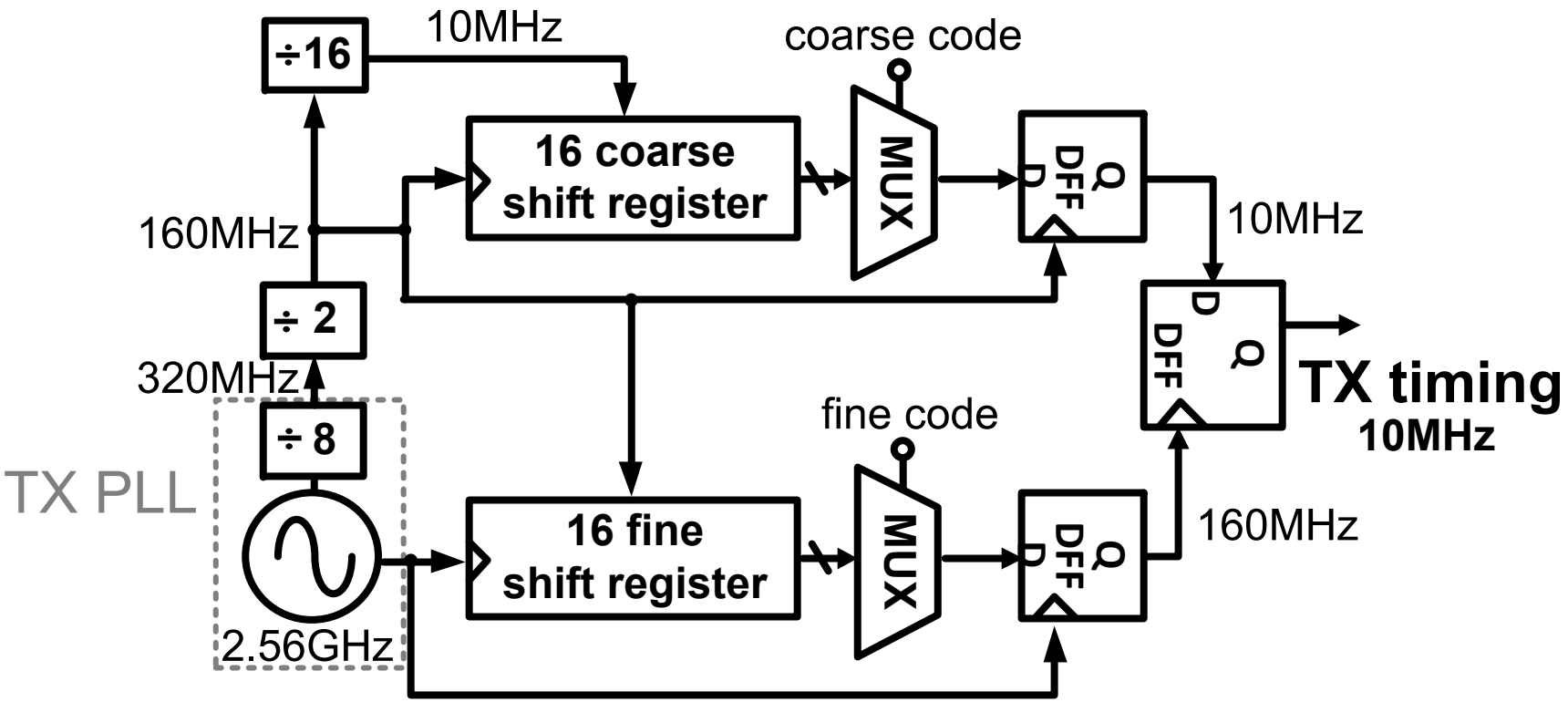
Sub-Ranging Shift Register Planning



Drawback: size, power

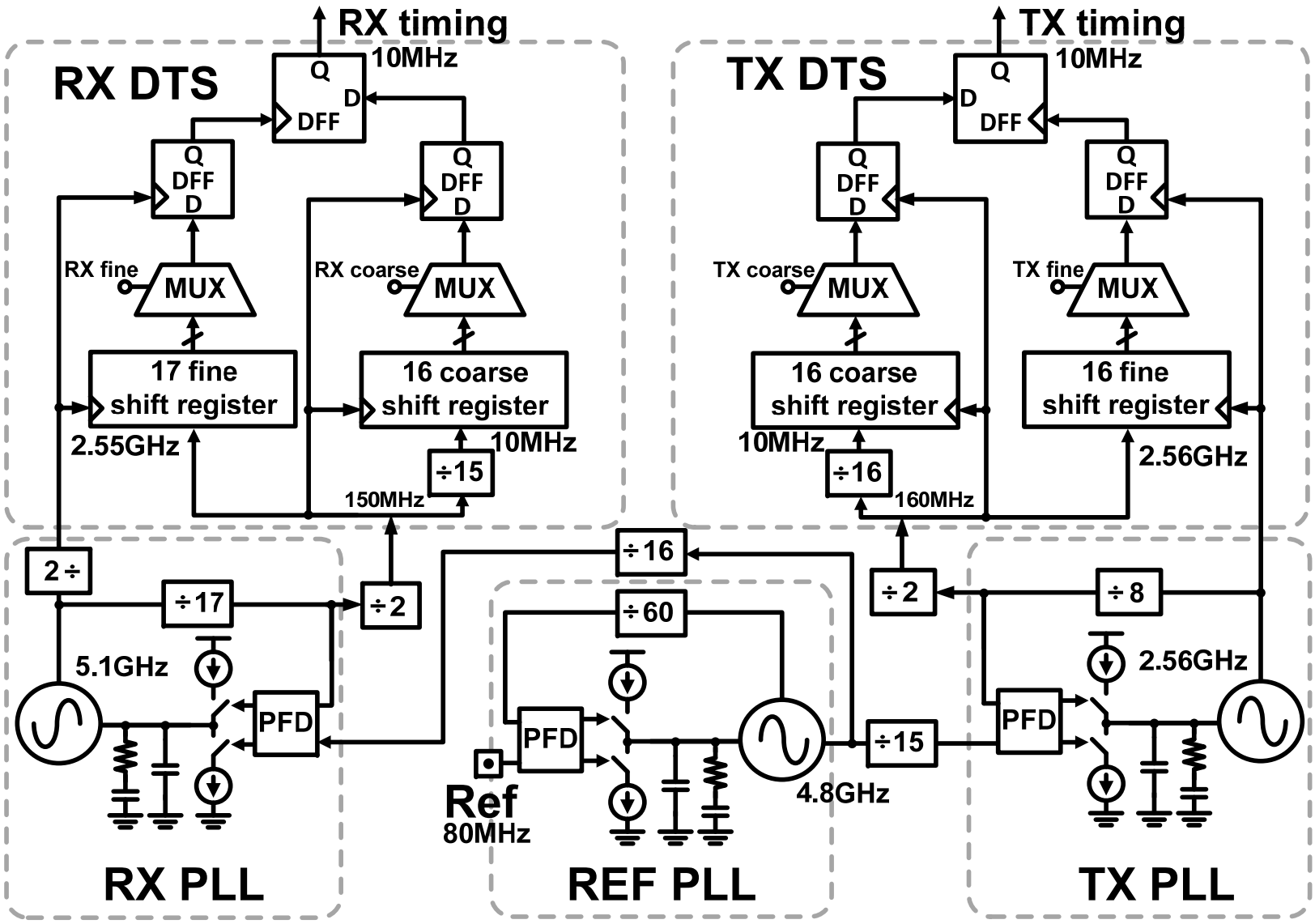
Drawback: area, power, phase mismatch

Sub-Ranging Shift Register Planning



	Straightforward	Sub-ranging approach
No. D-Flip Flop in SR.	256	32 (16+16)
Maximum clock loading	Drive 256 DFFs	Drive 16 DFFs
Input number of MUX	256	32 (16+16)

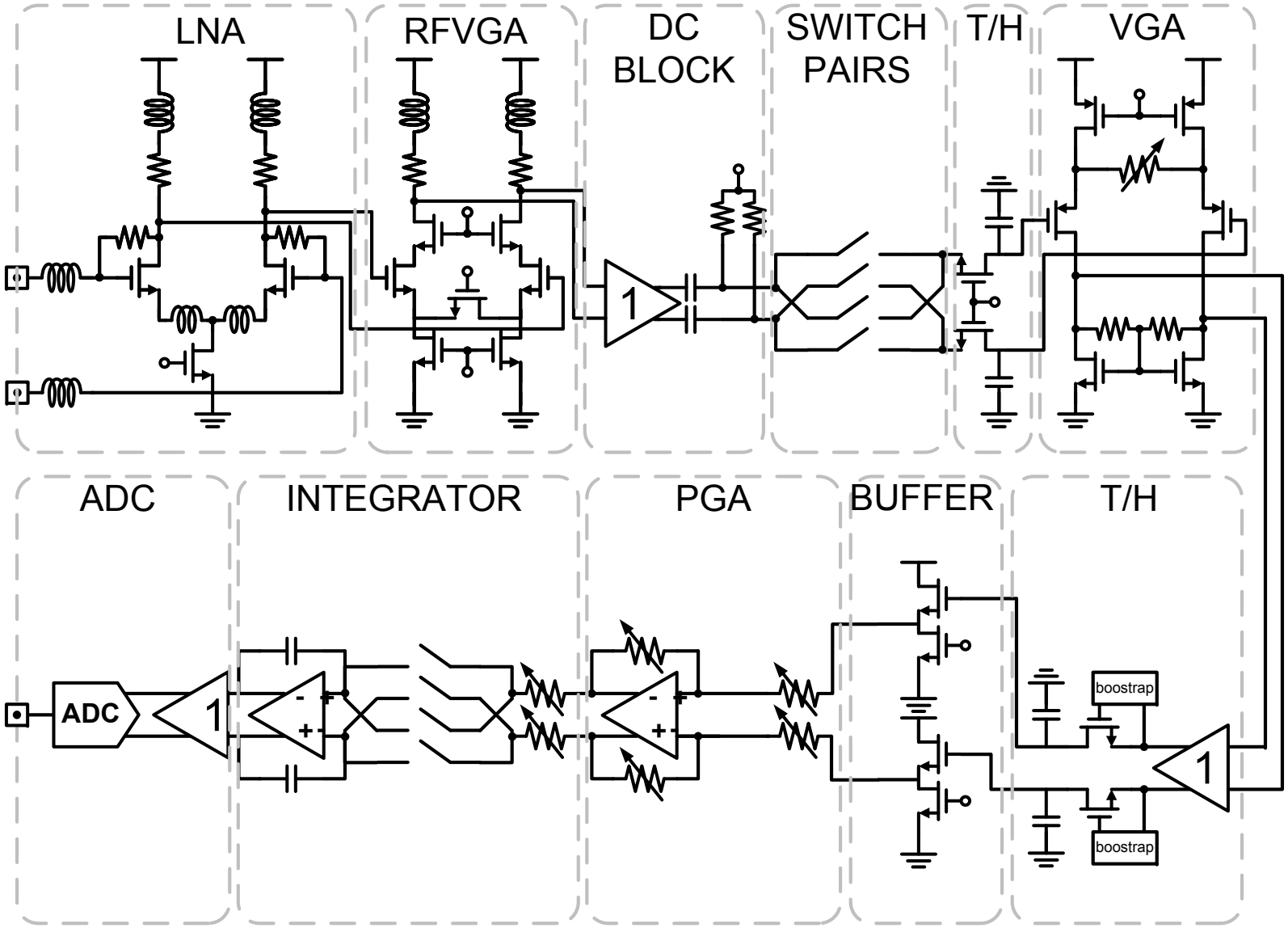
Proposed Frequency-Defined Vernier DTC



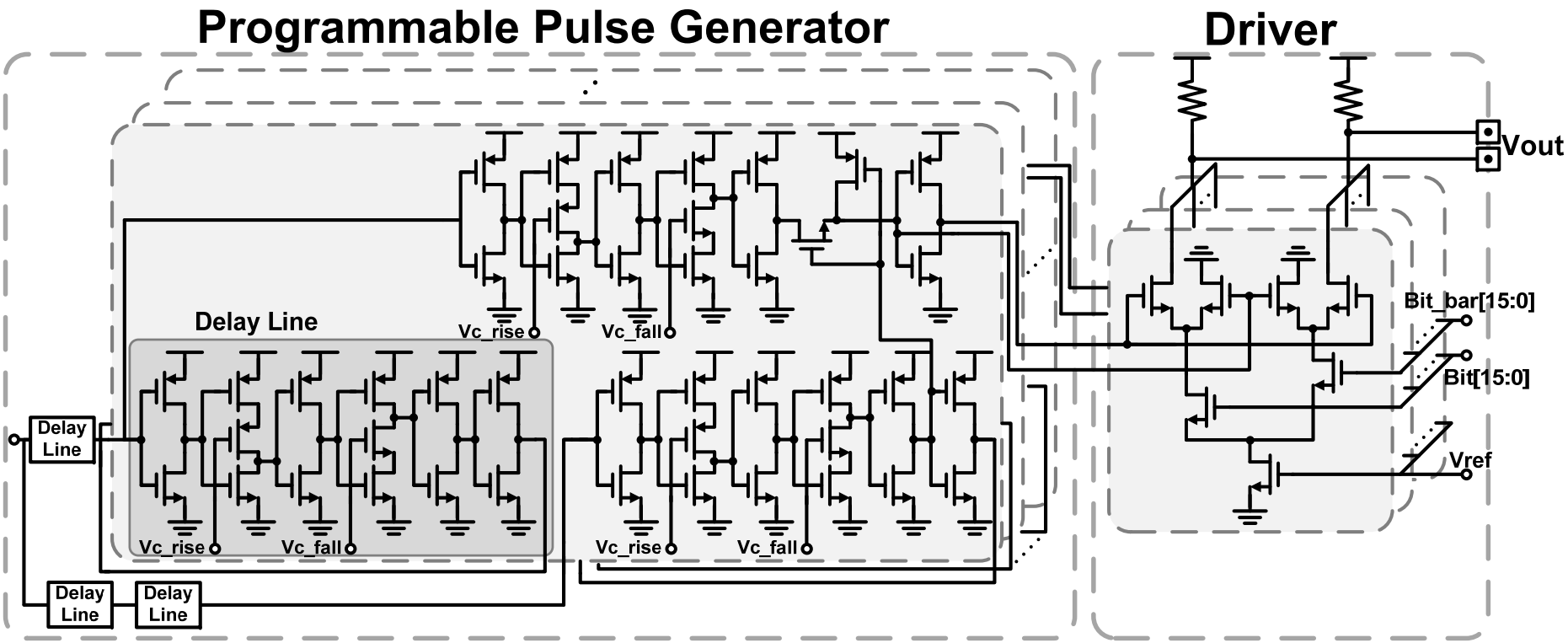
Outline

- Introduction
- Implemented direct-sampling radars
- Proposed frequency-defined Vernier DTC
- Circuit schematic of radar transceiver
- Measurement results
- Conclusions

Implemented Receiver Circuit



Implemented Transmitter Circuit



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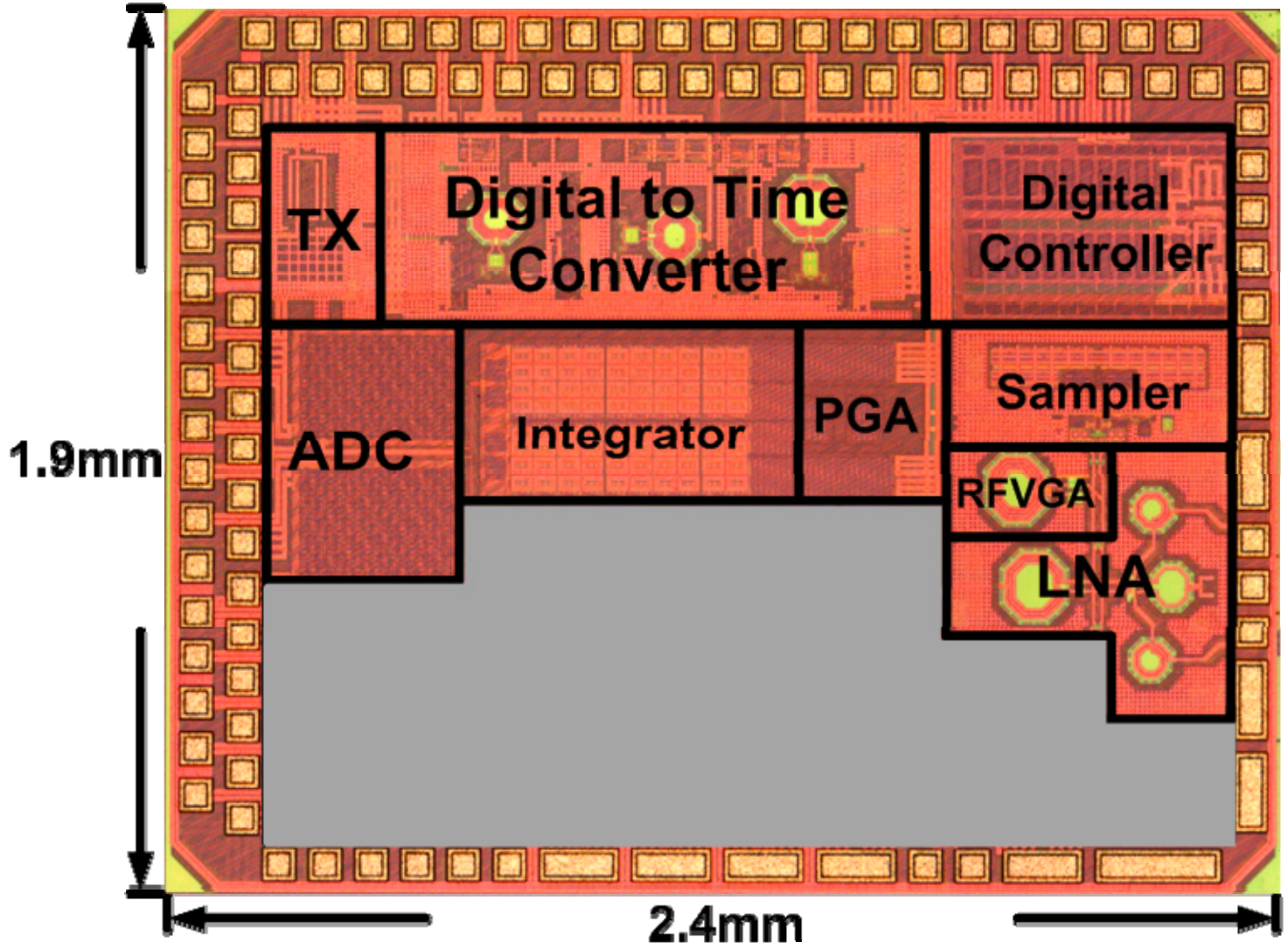
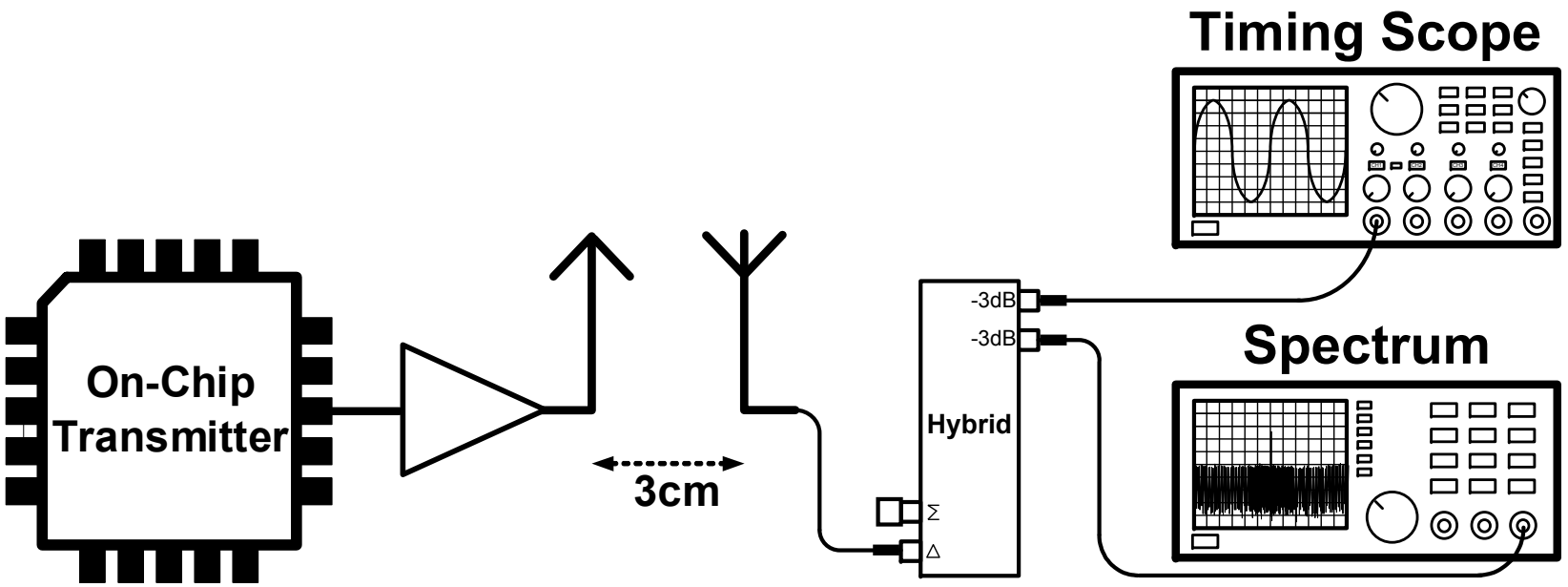
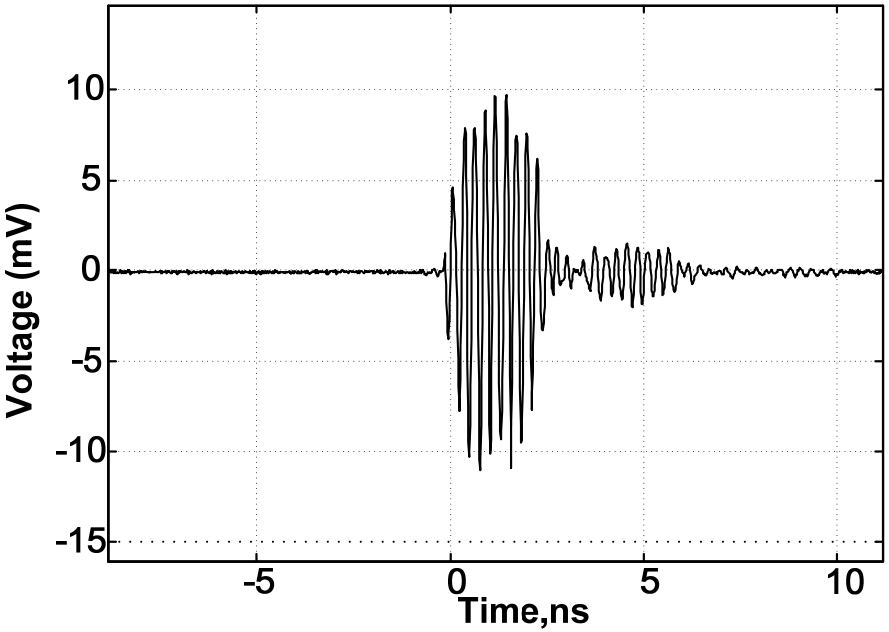
Chip Microphotograph

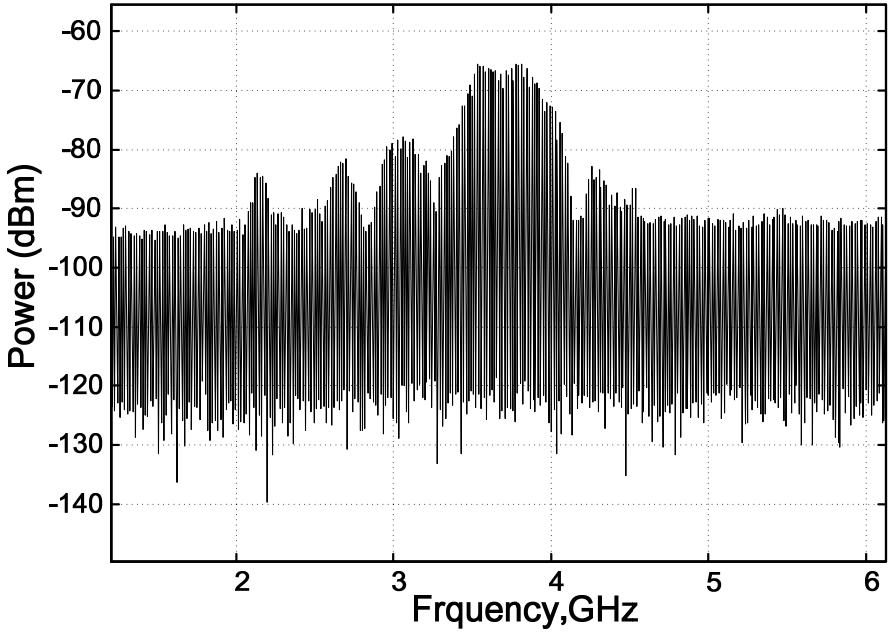


Transmitter Measurement

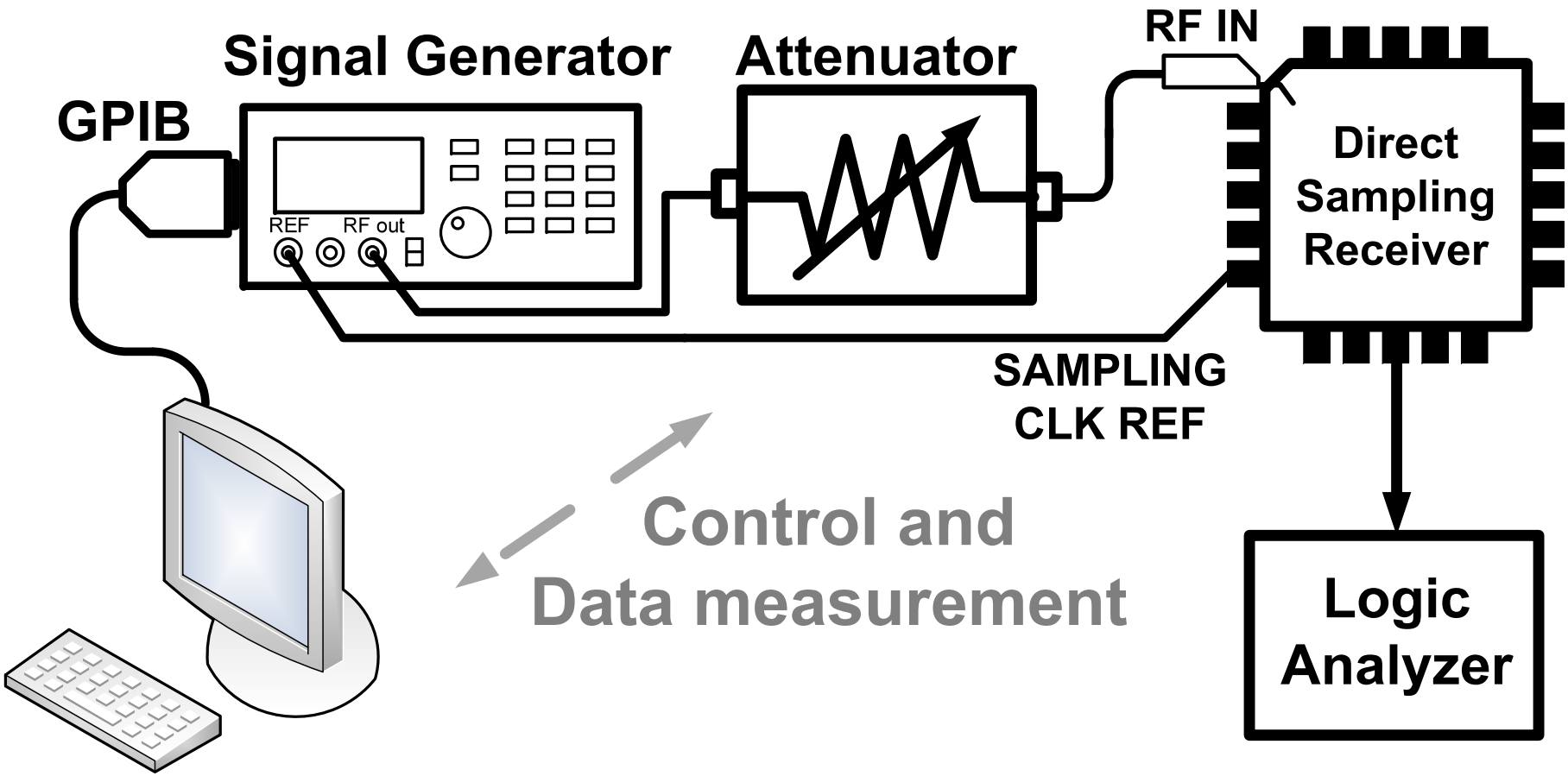


Transmitter Measurement

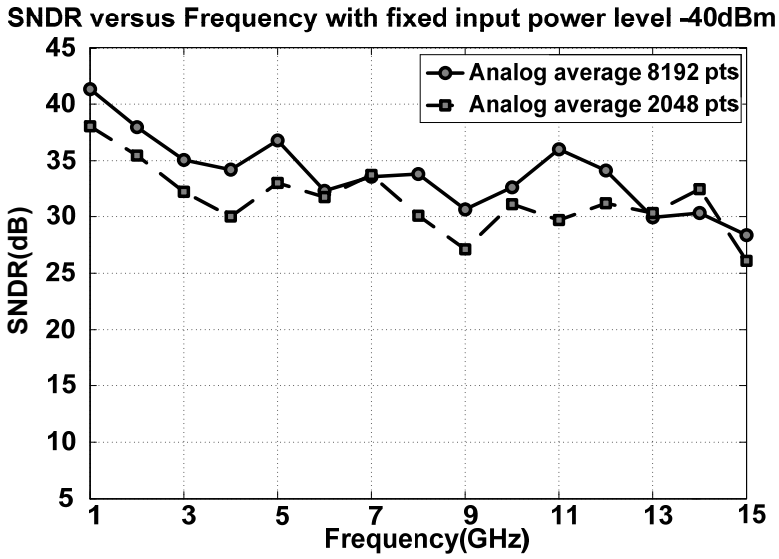


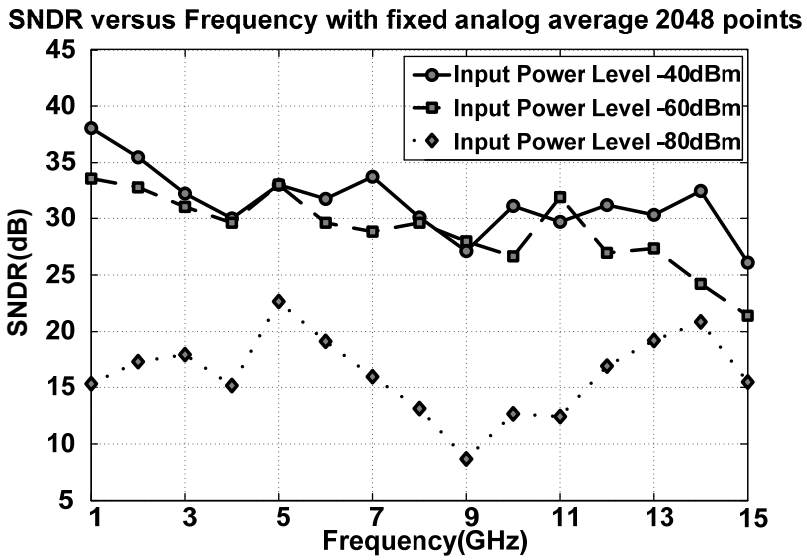


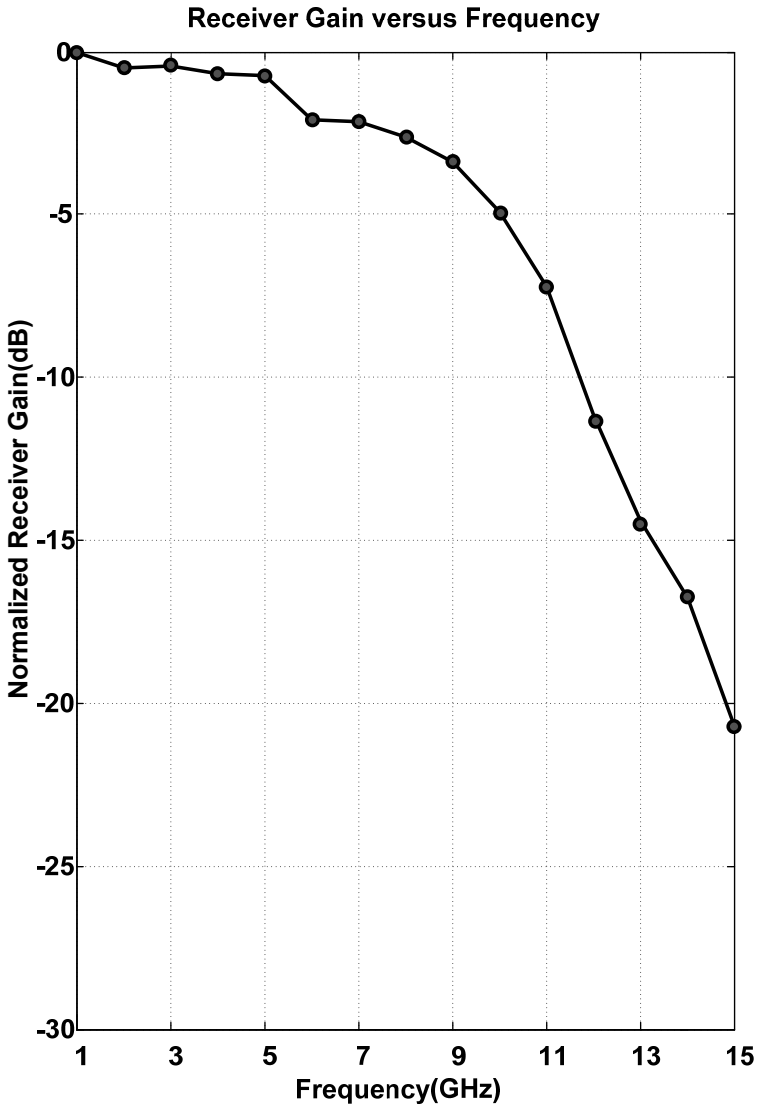
Receiver Measurement



Receiver Measurement

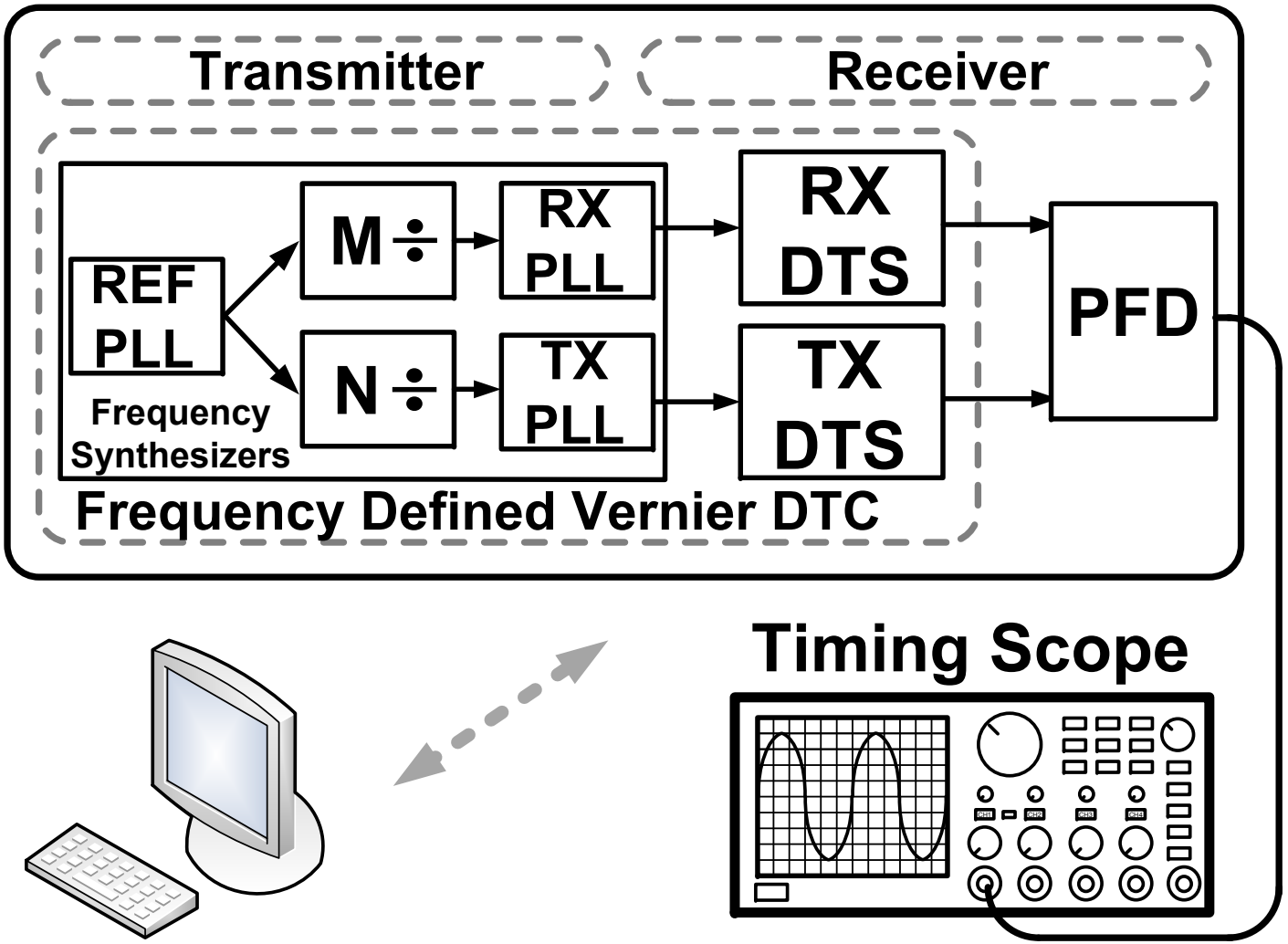




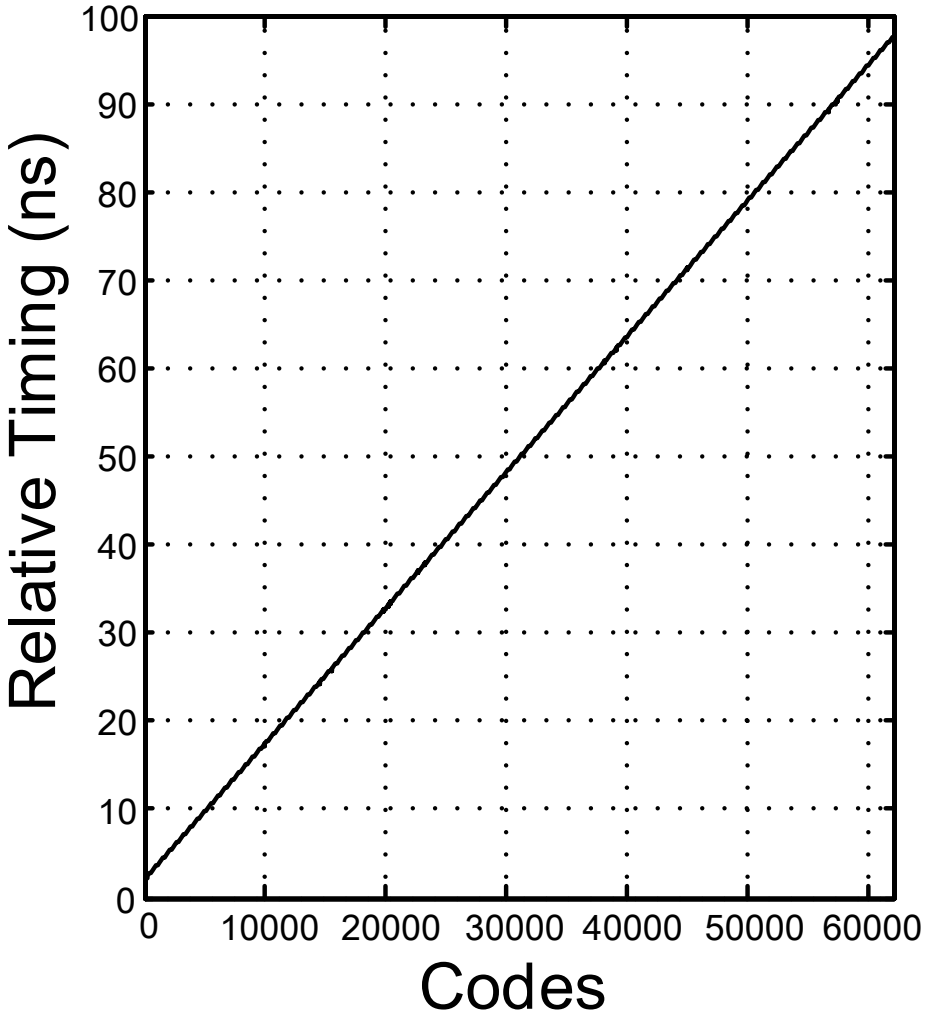


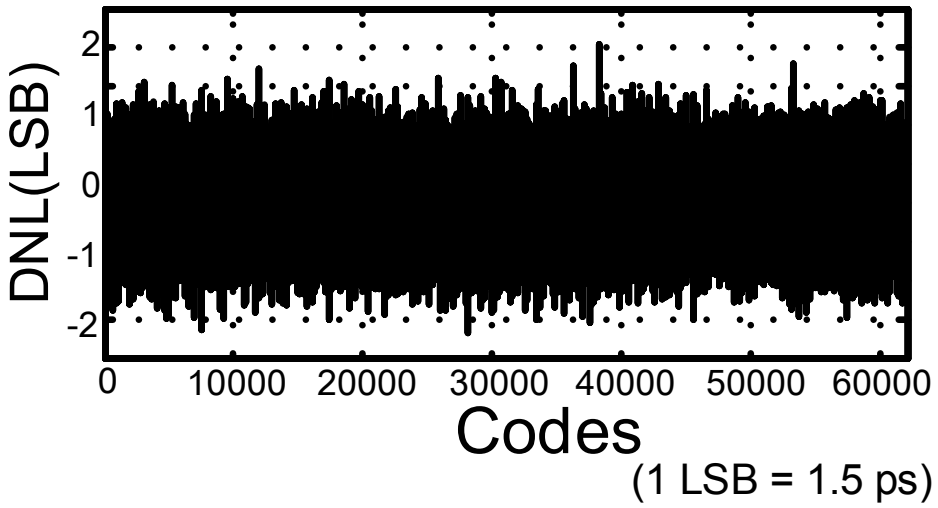
DTC Measurement

Implemented Radar Chip

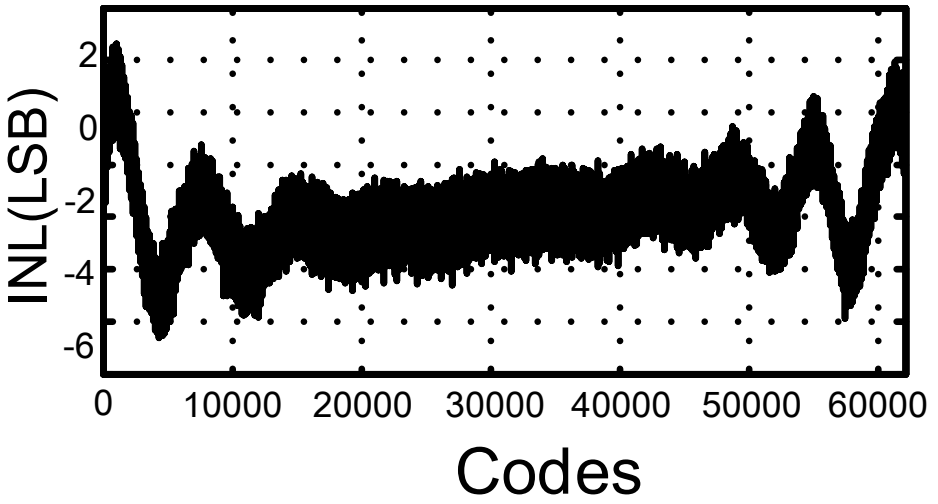


DTC Measurement



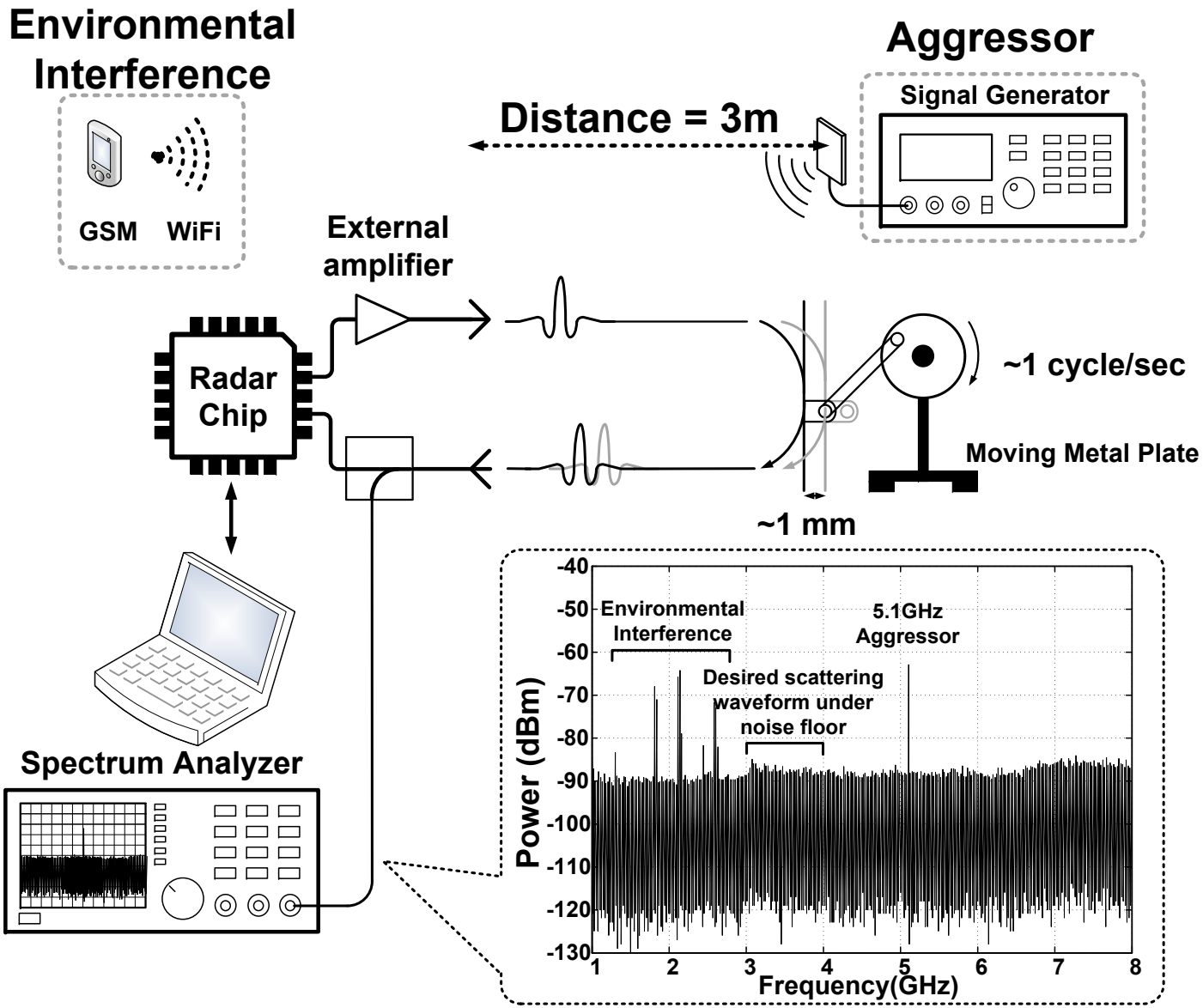


(1 LSB = 1.5 ps)

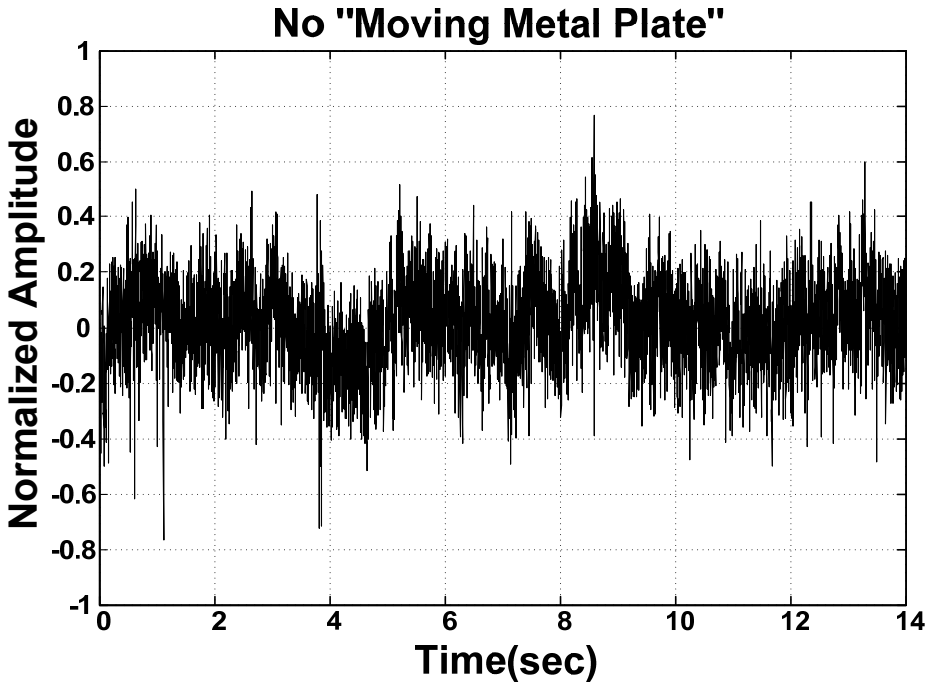


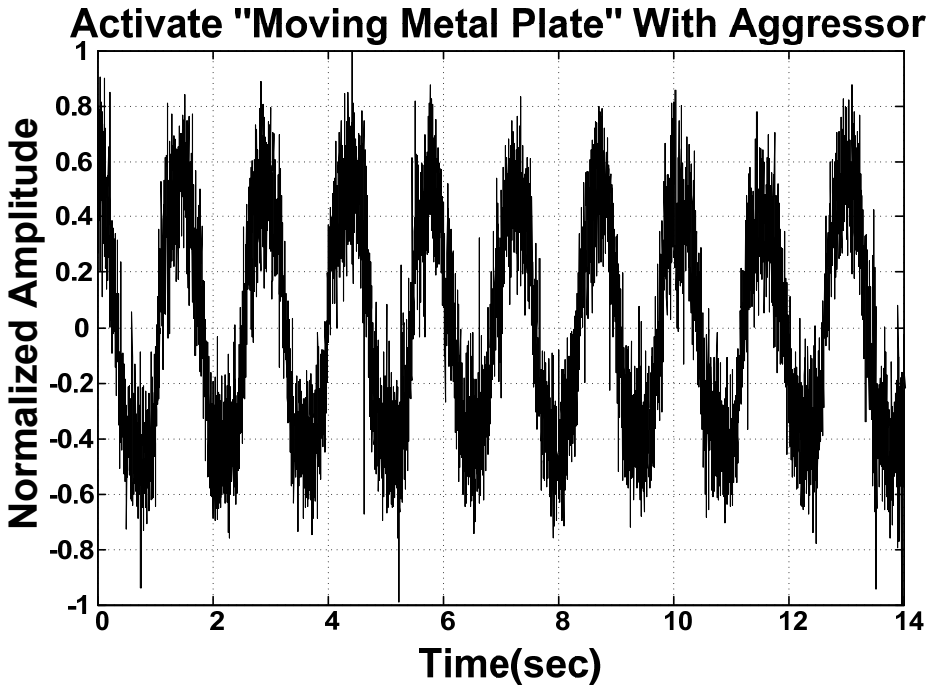
(1 LSB = 1.5 ps)

Wireless Measurement



Wireless Measurement





Performance of Radar Transceiver

Receiver And Transmitter Signal Path Circuitry	
Receiver gain bandwidth (-3dB)	8GHz
Receiver gain bandwidth (-10dB)	12GHz
MAX Receiver SNDR	>40dB
MAX SNR improvement (Theory)	48dB
ADC resolution/ENOB	8bit/7.3bit
Minimum Pulse Bandwidth (@3.8GHz)	17.5%
Current Consumption@1V	
RF front-end (LNA to S&H)	33.5mA
Analog blocks (include PGA, Integrator)	7.5mA
ADC	0.2mA
Frequency-defined Vernier DTC	44.5mA
Transmitter circuitry	0.5mA
Digital Controller and IO	2mA
Total	88.2mA

Comparison Table of DTCs

	ISSCC'13	VLSI'11	This work
Architecture	ECI	ECI	Vernier
Technology	65nm	0.18 μm	65nm
Die Area(Transceiver)(mm^2)	1.3x1.4	5.4X9.1	2 (core)
Supply Voltage	1V	1.8V	1V
Reference Clock Frequency	10MHz	12.5MHz	80MHz
Pulse Repetition Rate	10MHz	12.5MHz	10MHz
Timing resolution (1psec= 0.15mm)	6.25ps (0.937mm)	50ps (7.5mm)	1.5ps (0.225mm)
Maximum Scanning Range	100ns(15m)	80ns(12m)	100ns(15m)
DNL (LSB)	+1/-0.8		+2/-2
INL (LSB)	+15/0		+2/-6
Response Time	PLL defined	PLL defined	instant

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Conclusion

- A highly-integrated, impulse radar system has been implemented in a 65nm CMOS technology.
- A Digital-to-Time converter with dedicated resolution, instantaneous response time and insensitive PVT variation is proposed.
- A design approach is offered to attain the THz-like scanning resolution application.

Acknowledgement

- Thanks for partially support from
  - NTHU-MediaTek Joint Lab
  - National Science Council

- Our thanks to
  - Prof. Ta-Shun Chu's group members, NTHU